

The IBM logo, consisting of the letters 'IBM' in a bold, sans-serif font with horizontal stripes, is positioned at the top center of the slide. A registered trademark symbol (®) is located to the right of the letters.

# PowerPC<sup>TM</sup> 970:

First in a new family of 64-bit high performance  
PowerPC processors



**Peter Sandon**  
**Senior PowerPC Processor Architect**  
**IBM Microelectronics**

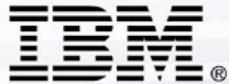
All information in these materials is subject to change without notice. All information is provided on an "as is" basis, without any warranty of any kind.

© Copyright IBM Corporation 2002. All rights reserved.

# PowerPC 970 Design Objectives and Overview



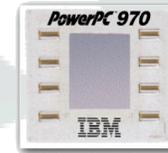
- Leverage architectural advantages of 64-bit POWER4™ for new generation of PowerPC processor
- Provide high performance general purpose processing through advanced superscalar design with multiple, pipelined execution units
- Enhance multimedia, graphics and data movement through hardware implementation of a SIMD processing facility
- Support the bandwidth demands of a highly superscalar and SIMD enhanced core through a high speed processor bus



# IBM PowerPC High Performance Roadmap

---

**64-Bit  
Microprocessors**



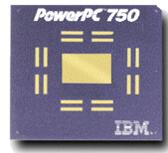
**PPC 970  
1.4 – 1.8 GHz**



**PPC 750FX  
500 - 1000MHz**



**PPC 750CXe  
300 - 600MHz**



**PPC 750  
300 - 500MHz**

**32-Bit  
Microprocessors**



Target frequencies are subject to change without notice.

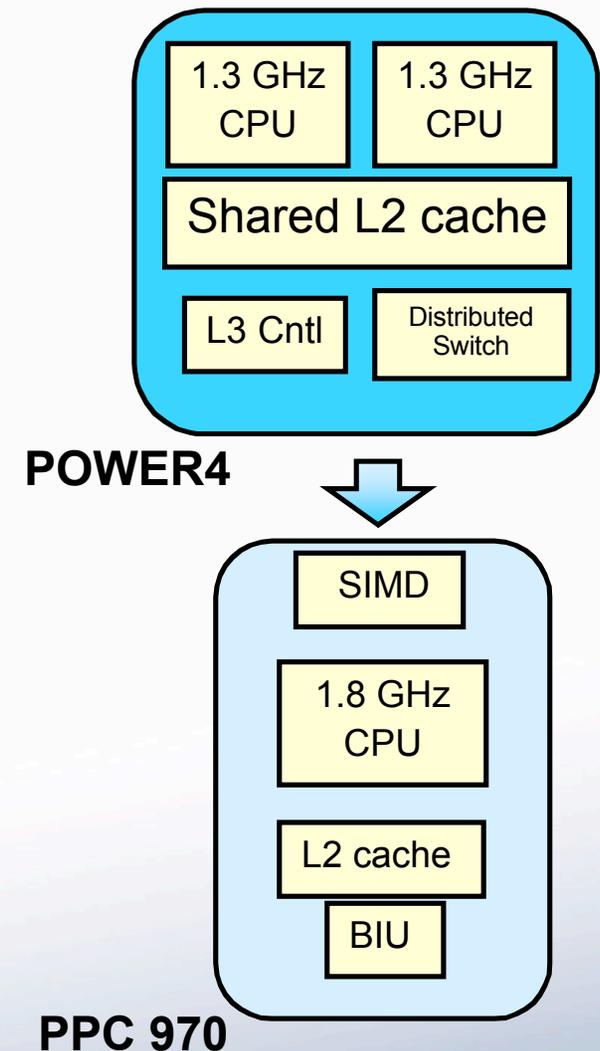
PowerPC 970 – MPF 2002



# Based on POWER4 Architecture

**PowerPC**

- **Winner MPR analyst's choice, 2001**
- **POWER4 design goals**
  - Balanced system/bus throughput design
  - SMP optimization
  - Native 32-bit compatibility
  - High frequency
- **PPC 970 implementation**
  - SIMD enhanced
  - Lower power
  - Smaller die
  - Single processor core



**IBM**

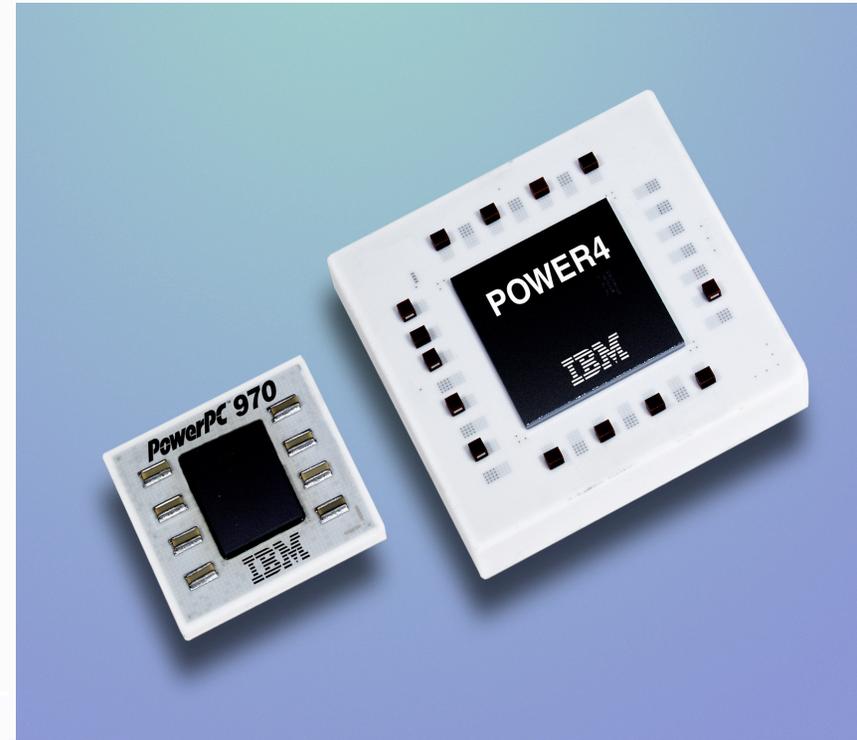
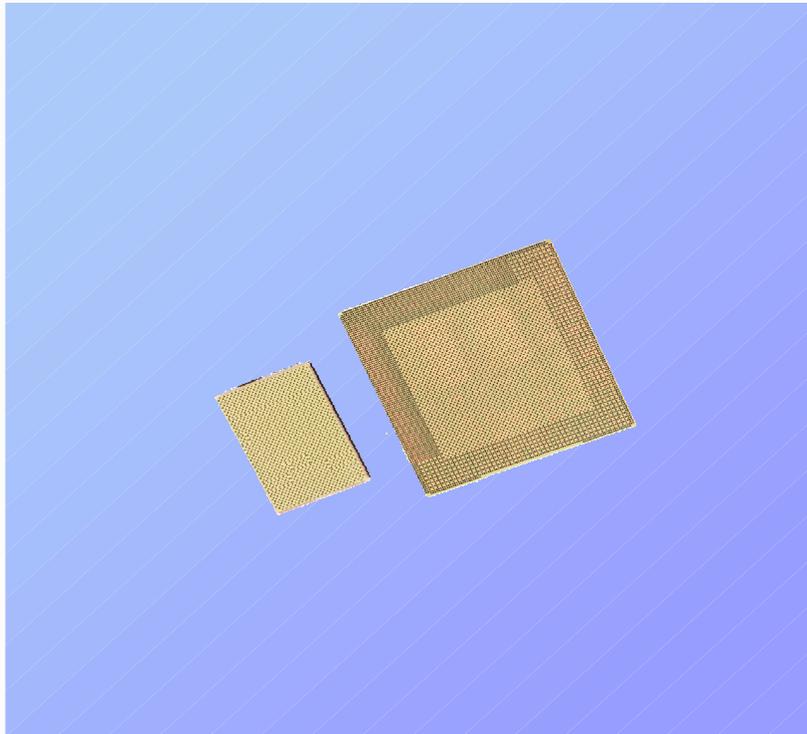
PowerPC 970 – MPF 2002

**Microelectronics**

# PPC 970 / POWER4 Size Comparison

---

**PowerPC**



**IBM**<sup>®</sup>

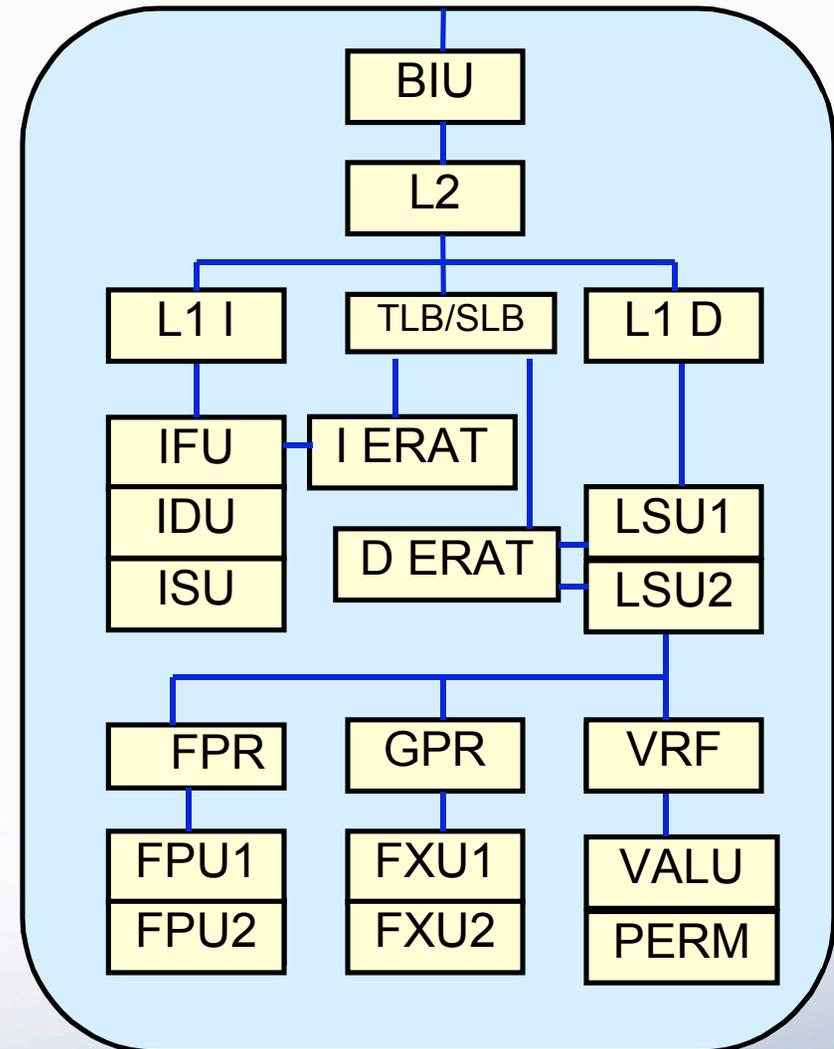
PowerPC 970 – MPF 2002

**Microelectronics**

# PPC 970 Features

**PowerPC**

- **Instruction pipe**
  - 64KB L1 Inst cache, direct mapped
  - 32 entry I buffer
  - 8 instructions fetch / cycle
- **Branch prediction**
  - Highly accurate dynamic prediction
- **Dispatch, issue**
  - 1 group (4 + branch) / cycle
  - Up to 20 active groups
  - Up to 8 issue / cycle
  - Over 200 instructions in flight
- **Data pipe**
  - 32 KB L1 Data cache, 2-way sa
  - 32 x 64b GPR, FPR
  - 32 x 128b VRF
  - 512KB L2 cache, 8-way sa
  - 8 data prefetch streams



**IBM**

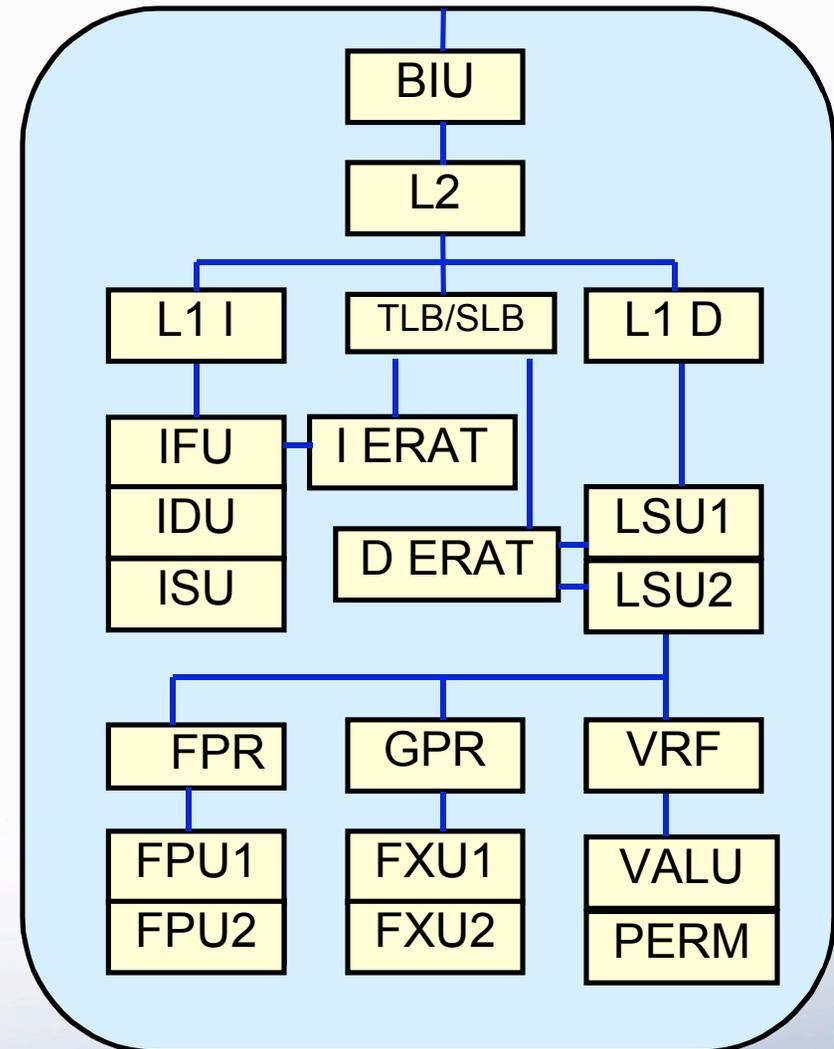
PowerPC 970 – MPF 2002

**Microelectronics**

# PPC 970 Features (cont.)

**PowerPC**

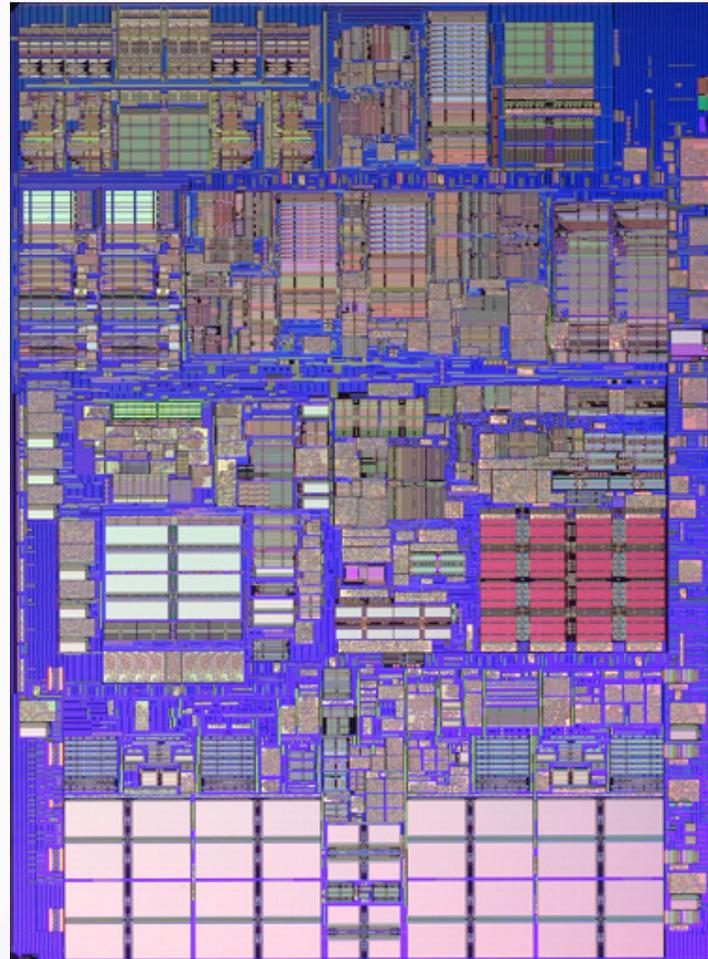
- Memory management
  - 64 entry SLB, fully associative
  - 256 x 4-way TLB
  - 64 x 2-way Inst and Data ERATs
  - Supports 42-bit real addresses
- Execution
  - 2 Load/store units
    - 64b for GPR, FPR
    - 128b for VRF
  - 2 Fixed point units
  - 2 IEEE floating point units
    - Single-, double-precision
  - 2 SIMD sub-units
    - VALU – 2 integer, float subunits
    - VPERM – permute
  - Branch unit
  - Condition register unit



# PowerPC 970 Die Overview

---

**PowerPC**



**IBM**<sup>®</sup>

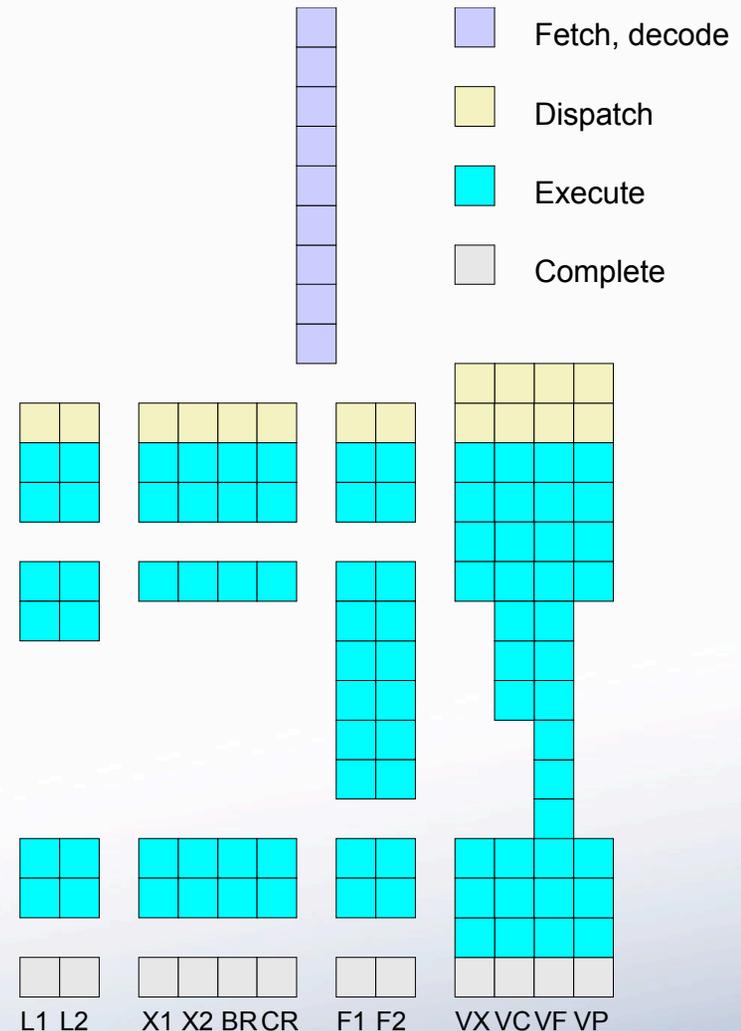
PowerPC 970 – MPF 2002

**Microelectronics**

# PPC 970 Pipeline



- Pipeline depths
  - 9 fetch, decode stages
  - 5 to 13 out of order execute stages
  - 2-3 dispatch, completion stages
- Pipeline width
  - Up to 8 fetched per cycle
  - Up to 5 dispatched per cycle
  - Up to 8 issued per cycle
  - 12 execution units
  - Up to 8 L1 D cache misses
  - Up to 5 completed per cycle
- Branch prediction
  - Up to 2 branches per cycle
  - 3 16K x 1 BHTs
  - Link stack, count cache



# 64-bit Processing - 32-bit Compatibility

---

**PowerPC**

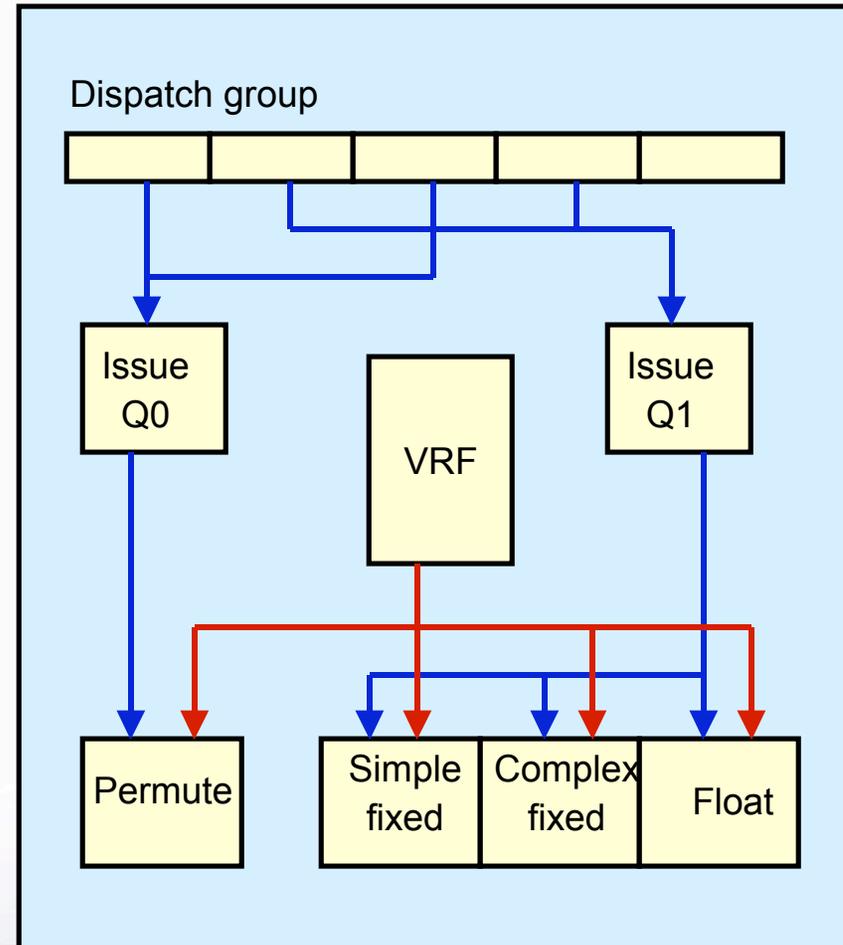
- **64-bit advantages**
  - Driven by need to address larger memory spaces
  - Performance advantage for data intensive applications
  - Enable new 64-bit solutions
- **Native 64-bit mode**
  - 64-bit fixed point processing
  - 64-bit effective addresses
  - 42-bit real addresses
  - Segment lookaside buffer caches segment table entries
- **Native 32-bit mode**
  - High word of all effective addresses are cleared
  - 32-bit PPC application code supported
  - First 16 entries of SLB are used as segment registers



# SIMD/Vector Engine

**PowerPC**

- Features
  - 162 specialized SIMD instructions
  - 128-bit data paths
  - 4-way SIMD single precision floating point (8 FP ops/cycle)
  - 4-way, 8-way, 16-way SIMD fixed point operations
- Two execution units
  - Permute unit
    - 16-entry issue queue
    - Permute, splat, merge
  - ALU – 3 subunits
    - 20-entry issue queue
    - Simple, complex fixed point
    - Floating point



**IBM**

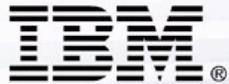
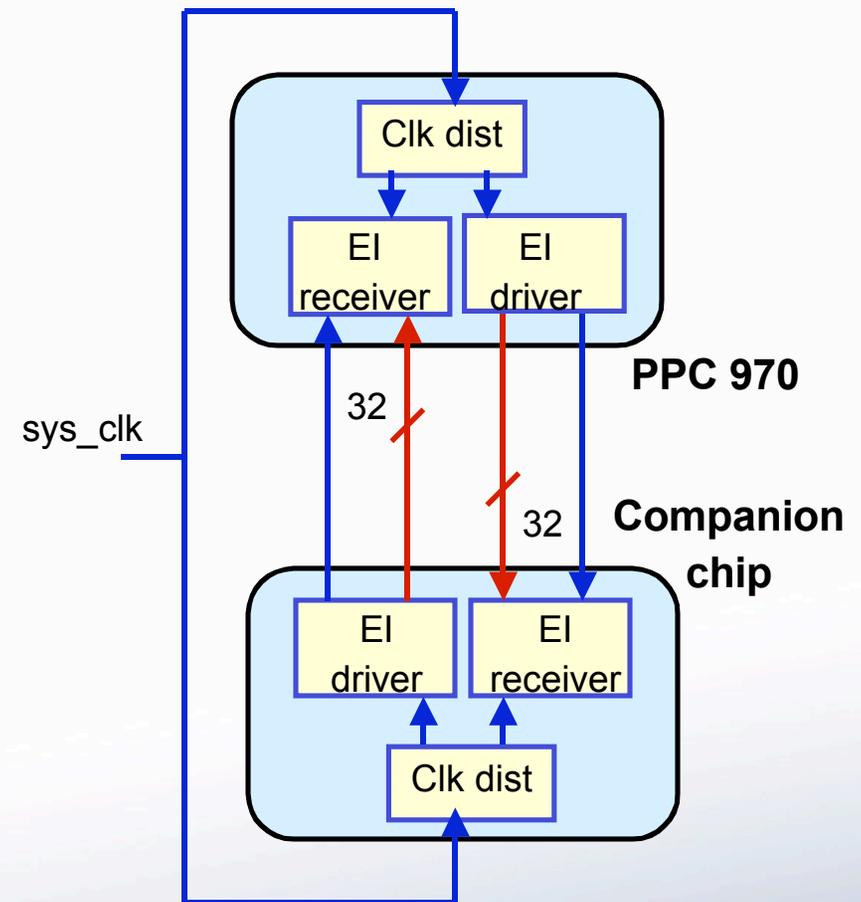
PowerPC 970 – MPF 2002

**Microelectronics**

# High Bandwidth Processor Bus

**PowerPC**

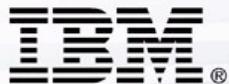
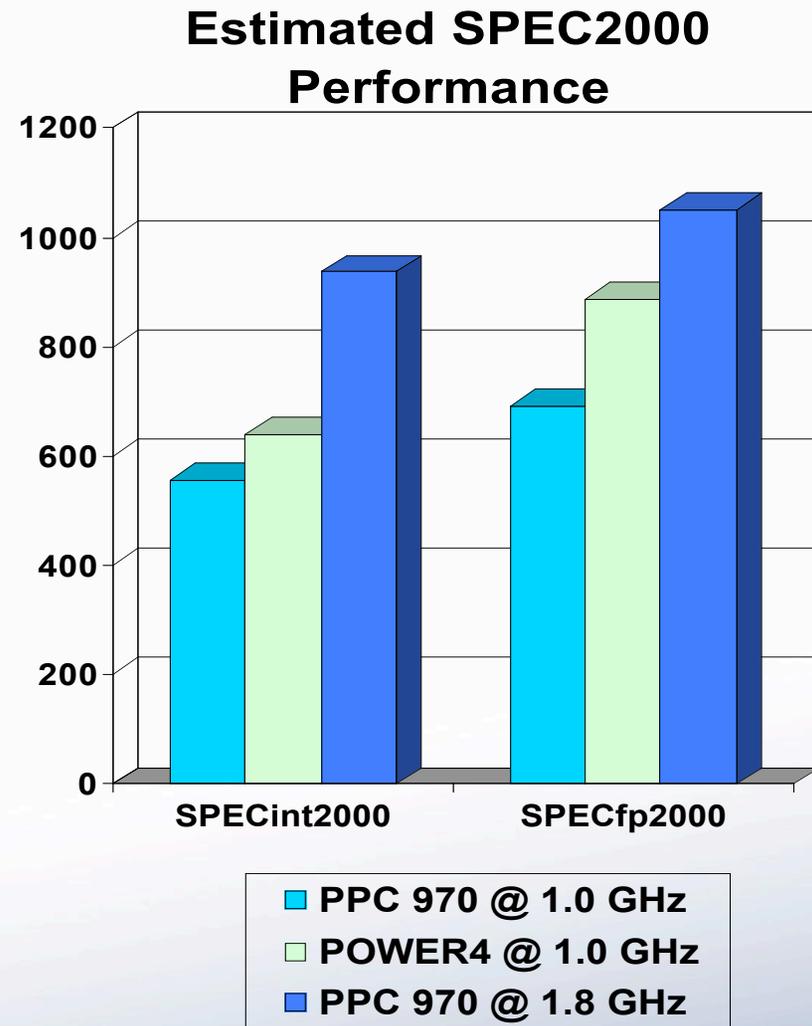
- Features
  - Two unidirectional busses
  - 32-bit read, 32-bit write
  - Point-to-point
  - Source synchronous
- Elastic interface
  - Allows multiple cycle wire delays between chips
  - Hardware deskews bit lines at POR
- Bus protocol
  - Address, control and data multiplexing
  - Sideband signals for snoop and ACK
  - Pipelined transactions
  - Out of order data
  - Coherency and sharing via snooping
  - Processor synchronization for SMP
- Up to 900 MHz bit rate achieves up to 6.4 GB/s useable bandwidth



# PPC 970 Performance



- **SPECint2000**
  - 937 @ 1.8 GHz\*
- **SPECfp2000**
  - 1051 @ 1.8 GHz\*
- **Dhrystone MIPS**
  - 5220 @ 1.8 GHz\*
  - 2.9 DMIPS / MHz
- **Additional Performance**
  - Peak scalar GFLOPS = 7.2
  - Peak SIMD GFLOPS = 14.4
  - RC5 : 18M keys/sec\*



\*All results are estimated performance;  
subject to change without notice

PowerPC 970 – MPF 2002

Microelectronics

# PowerPC 970 Parametrics

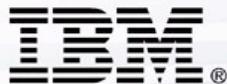


<b>Target Frequencies</b>	1.4 to 1.8 GHz
<b>Architecture</b>	64-bit PowerPC, 32-bit compatible
<b>Performance*</b>	937 SPECint2000 @ 1.8 GHz 1051 SPECfp2000 @ 1.8 GHz 5220 DMIPS @ 1.8 GHz (2.9 DMIPS/MHz)
<b>Caches</b>	64KB, I cache, w/parity 32KB, D cache, w/parity 512KB, L2 cache, w/ECC
<b>Voltages</b>	1.3V core logic and I/Os
<b>Typical Power Dissipation*</b>	42W @ 1.8 GHz, 1.3v 19W @ 1.2 GHz, 1.1v
<b>Package</b>	25x25mm CBGA 576 pins on 1mm pitch (161 signals)
<b>Technology</b>	0.13µm, CMOS w/ SOI 8 levels of copper interconnect
<b>Target Schedule*</b>	Samples 2Q 2003, Production 2H 2003

\*Estimation only; subject to change without notice.

Target frequencies are subject to change without notice.

Any performance data contained herein is preliminary and subject to change.



PowerPC 970 – MPF 2002

Microelectronics

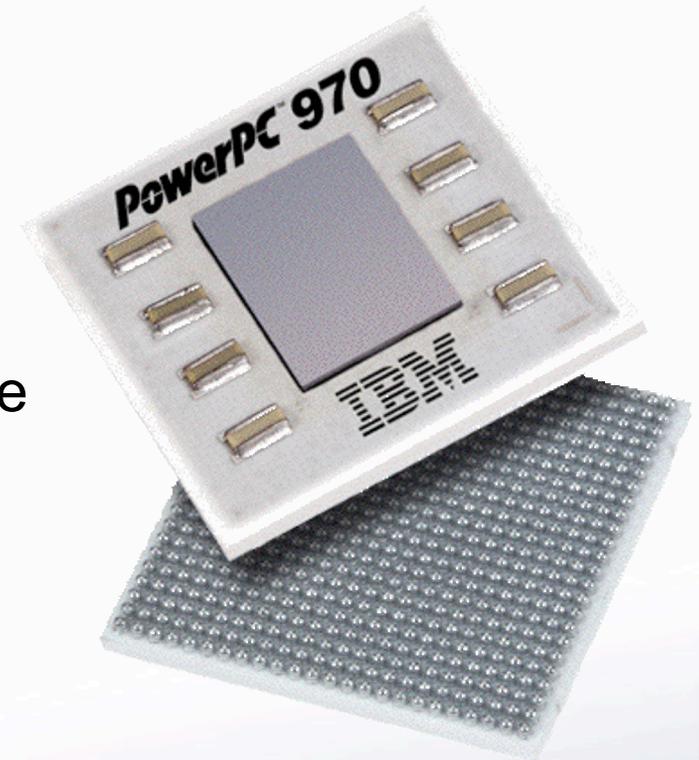
# Conclusion

---

**PowerPC**

## The IBM PowerPC 970 design constitutes

- An advanced 64-bit processor
- Derived from the POWER4 core
- Enhanced by a SIMD/Vector engine
- With a high bandwidth memory bus
- To achieve high performance on compute and bandwidth intensive applications



**[ibm.com/PowerPC](http://ibm.com/PowerPC)**

IBM, the IBM logo, POWER4, PowerPC, the PowerPC logo, and the PowerPC Architecture are trademarks of International Business Machines Corporation.

**IBM**<sup>®</sup>

**Microelectronics**

**(c) Copyright International Business Machines Corporation 2002.  
All Rights Reserved.  
Printed in the United States October 2002**

**The following are trademarks of International Business Machines Corporation in the United States, or other countries, or both.**

<b>IBM</b>	<b>IBM Logo</b>	<b>PowerPC</b>	<b>PowerPC Logo</b>
<b>POWER4</b>	<b>PowerPC 750</b>	<b>PowerPC 750CX</b>	<b>PowerPC 750CXe</b>
<b>PowerPC 750FX</b>	<b>PowerPC 970</b>		

**Other company, product and service names may be trademarks or service marks of others.**

**All information contained in this document is subject to change without notice. The products described in this document are NOT intended for use in applications such as implantation, life support, or other hazardous uses where malfunction could result in death, bodily injury, or catastrophic property damage. The information contained in this document does not affect or change IBM product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. All information contained in this document was obtained in specific environments, and is presented as an illustration. The results obtained in other operating environments may vary.**

**While the information contained herein is believed to be accurate, such information is preliminary, and should not be relied upon for accuracy or completeness, and no representations or warranties of accuracy or completeness are made.**

**THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN "AS IS" BASIS. In no event will IBM be liable for damages arising directly or indirectly from any use of the information contained in this document.**

**IBM Microelectronics Division  
1580 Route 52, Bldg. 504  
Hopewell Junction, NY 12533-6351**

**The IBM home page is <http://www.ibm.com>  
The IBM Microelectronics Division home page is <http://www.chips.ibm.com>**