IBM PowerPC® 750FX RISC Microprocessor

Datasheet for DD2.X Revisions

Preliminary Electrical Information

Version: 0.2

(Support for 750FX Design Revision Level DD2.X)

Preliminary - IBM Confidential

August 29, 2002

Printed in the United States of America August 2002

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Title_750FX_DS_DD2.X.fm.0.2
August 29, 2002
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Contents

Contents 3

List of Tables 5

List of Figures 7

1. General Information 9
1.1 Features 9
1.2 Design Level Considerations and Features 11
1.3 Processor Version Register 11
1.4 Part Number Information 12

2. Overview 13
2.1 Block Diagram 13
2.2 General Parameters 14

3. Electrical and Thermal Characteristics 15
3.1 DC Electrical Characteristics 15
3.2 AC Electrical Characteristics 18
3.3 Clock AC Specifications 19
3.4 Spread Spectrum Clock Generator (SSCG) 20
3.4.1 Design Considerations 20
3.6 60x Bus Output AC Specifications 24
3.6.1 IEEE 1149.1 AC Timing Specifications 27

4. Dimensions and Signal Assignments 30
4.1 Package 31
4.2 Microprocessor Ball Placement 32
4.3 Pinout Listings 33

5. System Design Information 41
5.1 Core Voltage Operation 41
5.2 Low Voltage Operation at Lower Frequency 41
5.2.1 Overview 41
5.2.2 Restrictions and Considerations for PLL Configuration 42
5.2.3 PLL Range[0:1] Definitions for Dual PLL Operation 43
5.2.4 PLL Configuration 44
5.3 PLL Power Supply Filtering 46
5.4 Decoupling Recommendations 50
5.5 Connection Recommendations 53
5.6 Output Buffer DC Impedance 53
5.6.1 Input-Output Usage 54
5.7 Thermal Management Information 59
5.7.1 Thermal Assist Unit 61

5.7.2 Internal Package Conduction Resistance 62
5.7.3 Adhesives and Thermal Interface Materials 63
5.8 Heat Sink Selection Example 64
5.9 Operational and Design Considerations 66
5.9.1 Level Protection 66
5.9.2 64 or 32-Bit Data Bus Mode 67
5.9.3 IIO Voltage Mode Selection 67

Revision Log 69

List of Tables

Table 1-1. 750FX Processor Version Register (PVR) 11
Table 2-1. 750FX General Parameters 14
Table 3-1. Absolute Maximum Ratings 15
Table 3-2. Recommended Operating Conditions 16
Table 3-3. Package Thermal Characteristics 16
Table 3-4. DC Electrical Specifications 17
Table 3-5. Power Consumption 18
Table 3-6. Clock AC Timing Specifications 19
Table 3-7. 60x Bus Input Timing Specifications 22
Table 3-8. 60x Bus Output AC Timing Specifications 24
Table 3-9. JTAG AC Timing Specifications (Independent of SYSCLK) 27
Table 4-1. List of Drawings with IBM Drawing Numbers 30
Table 4-2. Pinout Listing for the CBGA package 33
Table 4-3. Signal Listing for the CBGA Package 36
Table 4-4. Signal Locations 38
Table 4-5. Voltage and Ground Assignments 40
Table 5-1. PLL Range [0:1] Definitions for Dual PLL Operation 43
Table 5-2. 750FX Microprocessor PLL Configuration 44
Table 5-3. Sample PLL Power Supply Filtering Circuits 46
Table 5-4. Recommended Decoupling Capacitor Specifications 50
Table 5-5. Driver Impedance Characteristics 54
Table 5-6. Input-Output Usage 55
Table 5-7. Maximum Heatsink Weight Limit for the CBGA 60
Table 5-8. 750FX Heat Sink Vendors 61
Table 5-9. 750FX Thermal Interface and Adhesive Materials Vendors 64
Table 5-10. Summary of Mode Select 67

List of Figures

Figure 1-1. Part Number Legend 12
Figure 2-1. PowerPC 750FX RISC Microprocessor Block Diagram 13
Figure 3-1. SYSCLK Input Timing Diagram 19
Figure 3-2. Linear Sweep Modulation Profile 20
Figure 3-3. Input Timing Diagram 22
Figure 3-4. Mode Select Input Timing Diagram 23
Figure 3-5. Output Valid Timing Definition 25
Figure 3-6. Output Timing Diagram for PowerPC 750FX RISC Microprocessor 26
Figure 3-7. JTAG Clock Input Timing Diagram 28
Figure 3-8. TRST Timing Diagram 28
Figure 3-9. Boundary-Scan Timing Diagram 28
Figure 3-10. Test Access Port Timing Diagram 29
Figure 4-1. Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package 31
Figure 4-2. PowerPC 750FX Microprocessor Ball Placement 32
Figure 5-1. Single PLL Power Supply Filter Circuit with A1VDD Pin and A2VDD Pin Tied to GND 47
Figure 5-2. PLL Power Supply Filter Circuit with Two AVDD Pins and One Ferrite 48
Figure 5-3. Dual PLL Power Supply Filter Circuits 49
Figure 5-4. Orientation and Layout of the 750FX Decoupling Capacitors 51
Figure 5-5. 750FX Pin Locations: OV_{DD}, V_{DD}, GND, and Signal Pins 52
Figure 5-6. Driver Impedance Measurement 53
Figure 5-7. IBM RISCWatch™ JTAG to HRESET, TRST, and SRESET Signal Connector 59
Figure 5-8. Package Exploded Cross-Sectional View with Several Heat Sink Options 60
Figure 5-9. C4 Package with Heat Sink Mounted to a Printed-Circuit Board 62
Figure 5-10. Thermal Performance of Select Thermal Interface Material 63
Figure 5-11. Thermalloy #2328B Pin-Fin Heat Sink-to-Ambient Thermal Resistance vs. Airflow Velocity 65

1. General Information

The IBM PowerPC® 750FX RISC Microprocessor is a 32-bit implementation of the PowerPC family of reduced instruction set computer (RISC) microprocessors. This document contains pertinent physical and electrical characteristics of the PowerPC 750FX RISC Microprocessor Revision DD2.X Single Chip Modules (SCM). The IBM PowerPC 750FX RISC Microprocessor is also referred to as the 750FX throughout this document.

1.1 Features

This section summarizes the features of the 750FX implementation of the PowerPC Architecture™. Major features of the 750FX include the following:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Load/store unit
  - One cycle load or store cache access (byte, half-word, word, double-word)
  - Effective address generation
  - Hits under miss (one outstanding miss)
  - Miss under miss (one outstanding miss)
  - Single-cycle misaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big and little-endian byte addressing supported
  - Misaligned little-endian support in hardware
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, or floating-point)
  - 4-stage pipeline: fetch, dispatch, execute, and complete
  - Serialization control (predispatch, postdispatch, execution, serialization)
- Fixed-point units
  - Fixed-point unit 1 (FXU1): multiply, divide, shift, rotate, arithmetic, logical
  - Fixed-point unit 2 (FXU2): shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shift, rotate, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
  - Thirty-two 32-bit general purpose registers
- Floating-point unit
  - Support for IEEE-754 standard single and double-precision floating-point arithmetic
  - Optimized for single-precision multiply/add
  - Thirty-two, 64-bit floating point registers
  - Enhanced reciprocal estimates
  - 3-cycle latency, 1-cycle throughput, single-precision multiply-add
  - 3-cycle latency, 1-cycle throughput, double-precision add
  - 4-cycle latency, 2-cycle throughput, double-precision multiply-add
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions

- L1 Cache structure
  - 32K, 32-byte line, 8-way set associative instruction cache
  - 32K, 32-byte line, 8-way set associative data cache
  - Single-cycle cache access
  - Pseudo-LRU replacement
  - Copy-back or write-through data cache (on a page per page basis)
  - Parity on L1 tags and arrays
  - 3-state (MEI) memory coherency
  - Hardware support for data coherency
  - Non-blocking instruction cache (one outstanding miss)
  - Non-blocking data cache (two outstanding misses)
  - No snooping of instruction cache
- Memory management unit
  - 64 entry, 2-way set associative instruction TLB (total 128)
  - 64 entry, 2-way set associative data TLB (total 128)
  - Hardware reload for TLBs
  - 8 instruction BATs and 8 data BATs
  - Virtual memory support for up to 4 exabytes (2^{52}) virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Support for big/little-endian addressing
- Dual PLLs
  - Allows seamless frequency switching
- Level 2 (L2) cache
  - Internal L2 cache controller and 4K-entry tags: 512K data SRAMs
  - Two-way set-associative, supports locking by way
  - Copy-back or write-through data cache on a page basis, or for all L2
  - 64-byte sectored line size
  - L2 frequency at core speed
  - ECC protection on SRAM array
  - Parity on L2 tags
  - Supports up to 2 outstanding misses (1 data and 1 instruction)
  - Supports up to 2 outstanding misses (2 data)
- Power
  - Low power consumption with low voltage application at lower frequency
  - Dynamic power management
  - 3 static power save modes (doze, nap, and sleep)
- Bus interface
  - 32-bit address bus
  - 64-bit data bus (or 32-bit mode)
  - Enhanced 60x bus: pipelines back-to-back reads to a depth of 2
  - Core-to-bus frequency multipliers of 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 8.5x, 9x, 9.5x, 10x, 11x, 12x, 13x, 14x, 15x, 16x, 17x, 18x, 19x, and 20x supported
  - Supports 1.8V, 2.5V, or 3.3V I/O signals
- Reliability and serviceability
  - Parity checking on 60x busses
  - ECC checking on L2 cache
  - Parity on the L1 arrays
  - Parity on the L1 and L2 tags
- Testability
  - LSSD scan design
  - Powerful diagnostic and test interface through Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface

1.2 Design Level Considerations and Features

The 750FX supports several unique features including those listed below. The IBM application note *Differences between the PowerPC 750FX, 750, 750CX, and 750CXe Microprocessors* provides a more detailed explanation of these features.

- Provides a 64 or 32-bit Data Bus mode (per setup of $\overline{\text{TLBISYNC}}$ pin)
- Supports 1.8V, 2.5V, or 3.3V1 I/O signals

  Implementation Note: DD2.0 supports a limited use of the 3.3V I/O level (see DD2.x errata document).
- Includes all 60x bus pins on earlier PowerPC 750 designs with some added signals
- Enhanced 60x bus: pipelined read transactions
- Dual PLLs for additional power savings capabilities
- Four additional IBAT/DBAT registers
- New CBGA package with additional pins and depopulated footprint

1.3 Processor Version Register

The PowerPC 750FX RISC Microprocessor has the following Processor Version Register (PVR) values for the respective design revision levels.

The 750FX PVR is 7000, which is not used in any previous PowerPC processor design.

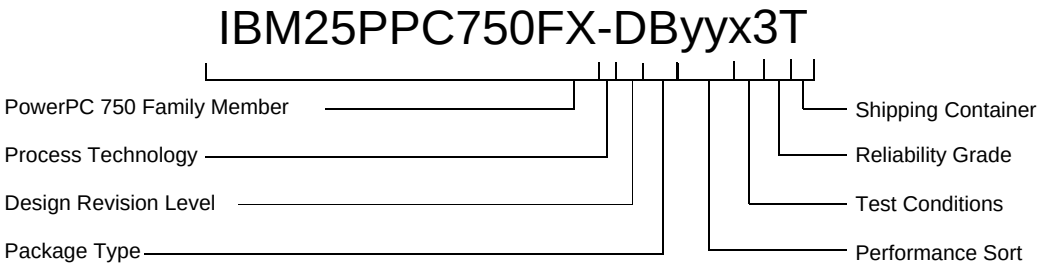
Table 1-1. 750FX Processor Version Register (PVR)

750FX Design Revision Level	750FX PVR	Notes
DD2.0	0x70000200	
DD2.1	0x70000201	
DD2.2	0x70000202	

1.

1.4 Part Number Information

Figure 1-1. Part Number Legend



Design Revision Level	D = DD2.0, E = DD2.1, F = DD2.2
Package Type	B = Ceramic Ball Grid Array
Performance Sort	01 = Nominal at 600MHz 05 = Nominal at 700MHz 10 = Nominal at 733MHz
Customer Sort	1 = 1.35 -1.45V @ 105°C 2 = Special Test Conditions
Reliability Grade	2 = Grade 2, < 25 FITS 3 = Grade 3, <100 FITS
Shipping Container	T = Tray

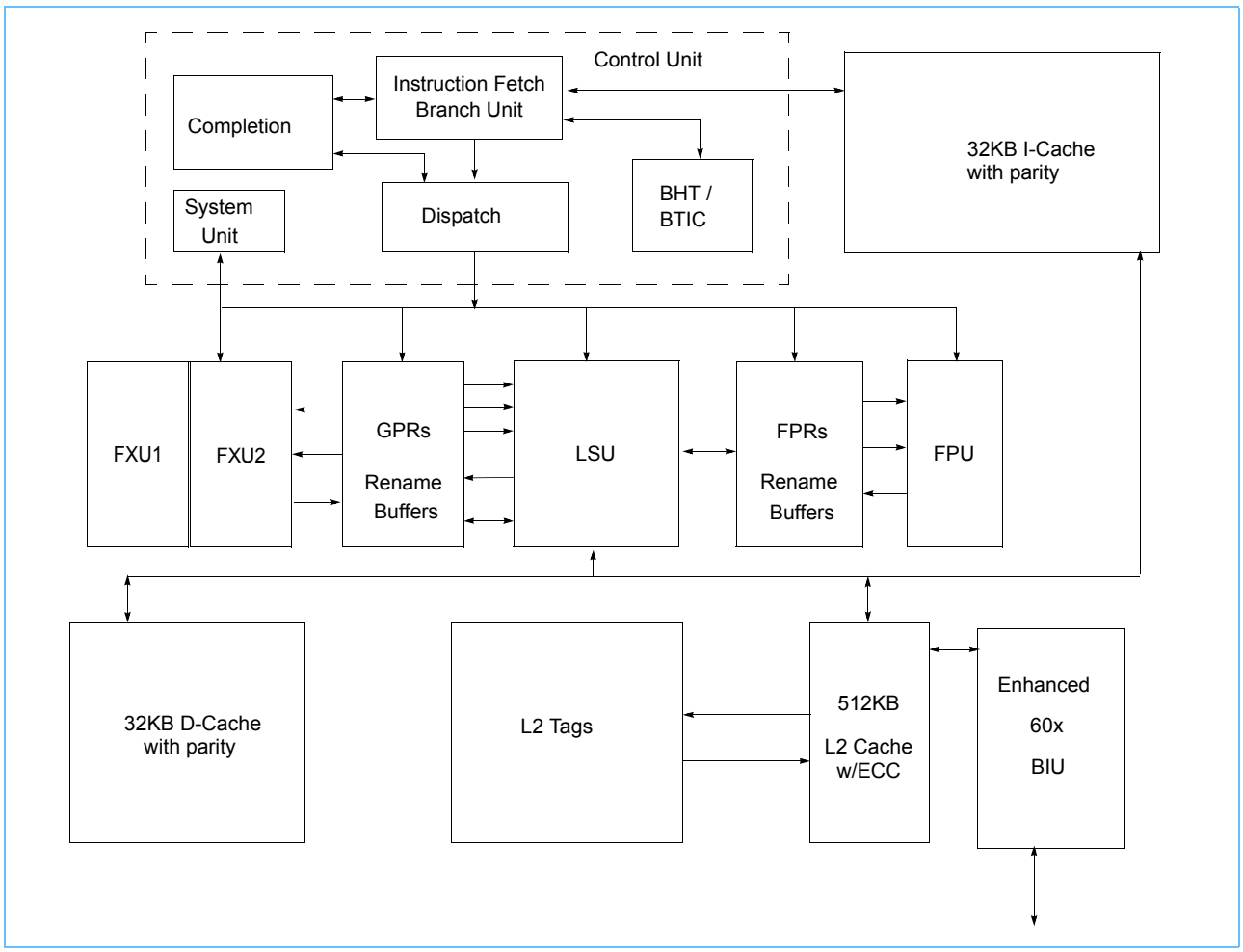
2. Overview

The PowerPC 750FX RISC Microprocessor, also called the 750FX, is targeted for high performance, low power systems using a 60x bus. The 750FX also includes an internal 512KB L2 cache with on-board Error Correction Circuitry (ECC).

2.1 Block Diagram

Figure 2-1 shows a block diagram of the PowerPC 750FX RISC Microprocessor.

Figure 2-1. PowerPC 750FX RISC Microprocessor Block Diagram



2.2 General Parameters

Table 2-1 provides a summary of the general parameters of the 750FX.

Table 2-1. 750FX General Parameters

Item	Description	Notes
Technology	0.13µm CSOI technology, six-layer metallization plus one level of local interconnect	
Die Size	34.3 sq. mm	
Transistor count	38 million - including L2 cache	
Logic design	Fully-static	
Package	292-pin ceramic ball grid array (CBGA) 21x21mm (1.0 mm pitch) 0.8 mm ball size	
Core power supply	1.4V ± 50 mV	1
I/O power supply	3.3V ± 165mV (BVSEL = 1, L1_TSTCLK = 0) or 2.5V ± 125mV (BVSEL = 1, L1_TSTCLK = 1) or 1.8V ± 100mV (BVSEL = 0, L1_TSTCLK = 1)	2

Note:

1. Lower core voltages are offered to allow slower operation at substantial power savings.
2. BVSEL =0, L1_TSTCLK = 0 is an INVALID condition.

3. Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the 750FX.

3.1 DC Electrical Characteristics

The tables in this section describe the DC electrical characteristics for the 750FX.

To find out more about...	See...
the absolute maximum ratings for the 750FX	Table 3-1 on page 15
the recommended operating conditions for the 750FX	Table 3-2 on page 16
the package thermal characteristics for the 750FX	Table 3-3 on page 16
DC electrical characteristics for the 750FX	Table 3-4 on page 17
the power consumption for the 750FX	Table 3-5 on page 18

Table 3-1. Absolute Maximum Ratings

Characteristic	Symbol	1.8V	2.5V	3.3V	Unit
Core supply voltage	V_{DD}	-0.3 to 1.6	-0.3 to 1.6	-0.3 to 1.6	V
PLL supply voltage	$A1V_{DD}$, $A2V_{DD}$	-0.3 to 1.6	-0.3 to 1.6	-0.3 to 1.6	V
60x bus supply voltage	OV_{DD}	-0.3 to 2.0	-0.3 to 2.75	-0.3 to 3.7	V
Input voltage	V_{IN}	-0.3 to 2.0	-0.3 to 2.75	-0.3 to 3.7	V
Storage temperature range	T_{STG}	-55 to 150	-55 to 150	-55 to 150	°C

Notes:

1. Functional and tested operating conditions are given in Table 3-2, “Recommended Operating Conditions” on page 16. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed above may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{IN} must not exceed OV_{DD} by more than 0.6V at any time, including during power-on reset.
3. **Caution:** OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 3.0V, except for up to 20ms during power on/off reset.
4. **Caution:** V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1.0V, except for up to 20ms during power up/down.
5. **Caution:** AV_{DD} must not exceed V_{DD} by more than 0.5V, except for up to 20ms during power up/down reset.

Table 3-2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit	Notes
Core supply voltage (full-on mode)	V_{DD}	1.35 to 1.45	V	1, 2
Low Voltage (Low Frequency Operation)	V_{DD}	1.2 Minimum	V	1, 2
PLL supply voltage	AV_{DD}	1.35 to 1.45	V	1,3
60x bus supply voltage (1.8V)	OV_{DD}	1.7 to 1.9	V	2
60x bus supply voltage (2.5V)	OV_{DD}	2.375 to 2.625	V	2
60x bus supply voltage (3.3V)	OV_{DD}	3.135 to 3.465	V	
Input voltage	V_{IN}	GND to OV_{DD}	V	2
Die-junction temperature	T_J	0 to 105	°C	

Notes:

1. Lower core voltages are supported to allow slower operation at substantial power savings. See, *750FX Datasheet Supplement for DD2.X Revisions*.
2. These are recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
3. AV_{DD} should be set to same value as V_{DD} for single voltage operation.

Table 3-3. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
CBGA package thermal resistance, junction-to-case thermal resistance (typical)	θ_{JC}	0.06	°C/W
CBGA package thermal resistance, junction-to-lead thermal resistance (typical)	θ_{JB}	7.6	°C/W

Note: θ_{JC} is the internal resistance from the junction to the back of the die. Refer to Section 5.7 “Thermal Management Information,” on page 59 for more information about thermal management.

Table 3-4. DC Electrical Specifications
See Table 3-2 on page 16 for recommended operating conditions.

Characteristic	Symbol	Voltage		Unit	Notes
		Min	Max		
Input high voltage (all inputs except SYSCLK)	$V_{IH\ (1.8V)}$	1.20	1.90	V	2, 4
	$V_{IH(2.5V)}$	1.70	2.625	V	2
	$V_{IH(3.3V)}$	2.00	3.465	V	2
Input low voltage (all inputs except SYSCLK)	$V_{IL(1.8V)}$	GND	0.60	V	4
	$V_{IL(2.5V)}$	GND	0.70	V	–
	$V_{IL(3.3V)}$	GND	0.80	V	–
SYSCLK input high voltage	$CV_{IH(1.8V)}$	1.20	1.90	V	–
	$CV_{IH(2.5V)}$	1.90	2.625	V	–
	$CV_{IH(3.3V)}$	2.0	3.465	V	–
SYSCLK input low voltage	$CV_{IL(1.8V)}$	GND	0.40	V	–
Input leakage current, V_{IN} = Applies to all OV_{DD} levels	I_{IN}	–	20	µA	3
Hi-Z (off state) leakage current, V_{IN} = Applies to all OV_{DD} levels	I_{TSI}	–	20	µA	3
Output high voltage, I_{OH} = –4mA	$V_{OH(1.8V)}$	1.30	–	V	–
	$V_{OH(2.5V)}$	2.00	–	V	–
	$V_{OH(3.3V)}$	2.40	–	V	–
Output low voltage, I_{OL} = 4mA	$V_{OL(1.8V, 2.5V)}$	–	0.4	V	–
Output low voltage, I_{OL} = 4mA	$V_{OL(3.3V)}$	–	0.4	V	–
Capacitance, V_{IN} =0 V, f = 1MHz	C_{IN}	–	5	pF	1

Notes:

1. Capacitance values are guaranteed by design and characterization, and are not tested.
2. Maximum input high voltage for short duration (not continuous operation).
3. Additional input current may be attributed to the Level Protection Keeper Lock circuitry. For details, see Section 5.9 on Page 66.
4. V_{IH} and V_{IL} minimum levels are set as a percentage of OV_{DD}. V_{IH} is 65% and V_{IL} is 35% respectively.

Note: For recommended operating conditions, see *Table 3-2 Recommended Operating Conditions* on page 16.

Table 3-5. Power Consumption
See Table 3-2 on page 16 for recommended operating conditions.

	Representative Processor Frequency				Unit	Notes
	400 MHz	600 MHz	700 MHz	733 MHz		
Full-On Mode						
Typical (V_{DD} = 1.4V) (85°C)	2.8	3.5	4.0	4.2	W	1, 3, 4
Maximum (V_{DD} = 1.45V) (105°C)	5.1	5.9	6.4	6.5	W	1, 2, 4
Low Voltage use (see supplement)						
Nap Mode						
Typical (V_{DD} = 1.4V) (50°C)	1.2	1.2	1.3	1.3	W	1, 5
Sleep Mode						
Typical (V_{DD} = 1.4V) (50°C)	1.1	1.1	1.1	1.1	W	1, 4

Notes:

1. These values apply for all valid 60x buses. The values do not include I/O Supply Power (OV_{DD}) or PLL/DLL supply power (AV_{DD}). OV_{DD} power is system dependent, but is typically <2% of V_{DD} power.
2. Maximum power is measured at VDD = 1.45V at105°C and assumes worst case instruction mix and process parameters.
3. Typical power is an estimate of the average value modeled in a system executing typical applications and benchmark sequences.
4. Guaranteed by design and characterization, and is not tested.
5. Power is measured, in nap mode at VDD = 1.4V at 50°C.

Note: For recommended operating conditions, see *Table 3-2 Recommended Operating Conditions* on page 16.

3.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the 750FX. After fabrication, parts are sorted by maximum processor core frequency as shown in Section 3.3 on Page 19, and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG(0-4) signals.

3.3 Clock AC Specifications

Table 3-6 provides the clock AC timing specifications as defined in Figure 3-1.

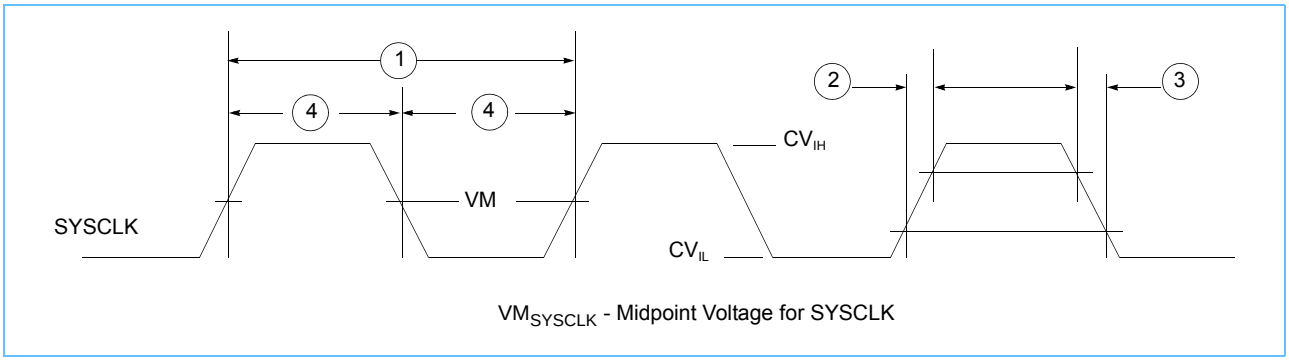
Table 3-6. Clock AC Timing Specifications
See Table 3-2 on page 16 for recommended operating conditions.[1,6]

Num	Characteristic	Value		Unit	Notes
		Min.	Max.		
	Processor frequency	400	733	MHz	7
	SYSCLK frequency	20	150	MHz	1, 6
1	SYSCLK cycle time	6.6	50	ns	
2, h3	SYSCLK rise and fall time (slew rate)	1.0	4.0	volt/ns	2, 3
4	SYSCLK duty cycle measured at 0.8V	25	75	%	3
VM_{SYSCLK}	Measurement Reference Voltage for SYSCLK (all I/O voltages)	0.65		V	8
	SYSCLK cycle-to-cycle jitter	–	±150	ps	4, 3
	Internal PLL relock time	–	100	µs	5

Notes:

1. **Caution:** The SYSCLK frequency and the PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Table 5-2, “750FX Microprocessor PLL Configuration” on page 44 for valid PLL_CFG[0:4] settings.
2. Rise and fall times for the SYSCLK inputs are measured from 0.4 to 1.0V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. See *Section 3.4 Spread Spectrum Clock Generator (SSCG)* on page 20 for long term jitter.
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
6. For applications with SYSCLK frequencies above 150 MHz, contact IBM PowerPC Application Engineering.
7. Lower voltage/frequency operation: as specified in table *1-3 Maximum Frequency at Minimum Voltage*
8. This is the SYSCLK reference voltage for Clock, Input & Output timing calculation.

Figure 3-1. SYSCLK Input Timing Diagram



3.4 Spread Spectrum Clock Generator (SSCG)

3.4.1 Design Considerations

When designing with the SSCG, there are a number of design issues that must be taken into account.

SSCG creates a controlled amount of long-term jitter. In order for a receiving PLL in the 750FX to operate in this environment, it must be able to accurately track the SSCG clock jitter.

The accuracy to which the 750FX PLL can track the SSCG clock is referred to as tracking skew. When performing system timing analysis, the tracking skew must be added or subtracted to the I/O timing specifications because the tracking skew appears as a static phase error between the internal PLL and the SSCG clock.

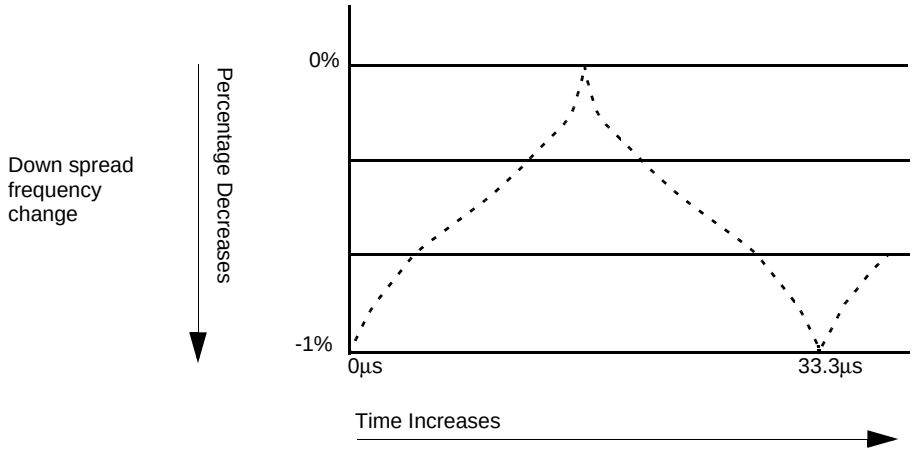
To minimize the impact on I/O timings the following SSCG configuration is recommended:

The following SSCG configuration is recommended:

- - Down spread mode, less than or equal to 1% of the maximum frequency
- - A modulation frequency of 30kHz
- - Linear sweep modulation or “Hershey Kiss™1” (as in a Lexmark2 profile) modulation profile as shown in *Figure 3-2* on page 20.

In this configuration the tracking skew is less than 100ps.

Figure 3-2. Linear Sweep Modulation Profile



1. Hershey Kiss is a trademark of Hershey Foods Corporation.
2. See patent 5,631,920.

3.5 60x Bus Input AC Specifications

To find out more about...	See...
the absolute maximum ratings for the 750FX	*Table 3-1* on page 15
the recommended operating conditions for the 750FX	*Table 3-2* on page 16
the package thermal characteristics for the 750FX	*Table 3-3* on page 16
DC electrical characteristics for the 750FX	*Table 3-4* on page 17
the power consumption for the 750FX	*Table 3-5* on page 18
60x bus input AC timing specifications	*Table 3-7* on page 22 provides the 60x bus input AC timing specifications for the 750FX as defined in *Figure 3-3* on page 22 and *Figure 3-4* on page 23

Table 3-7. 60x Bus Input Timing Specifications
See *Table 3-2* on page 16 for operating conditions.[1,5]

Num	Characteristic	1.8V Mode		2.5V Mode		3.3V Mode		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
10a	All inputs valid to SYSCLK (input setup)	1.0	—	1.5		1.8	—	ns	—
10b	INT_, SMI_, MCP, TBEN and TLBISYNC (input setup)	1.5		1.5		1.8			
10c	Mode select input setup to $\overline{\text{HRESET}}$ ($\overline{\text{QACK}}$, $\overline{\text{DRTRY}}$)	8	—	8	—	8	—	t_{sysclk}	2, 3, 4, 5
11a	SYSCLK to inputs invalid (input hold)	0.5	—	0.5	—	0.3	—	ns	
11b	INT_, SMI_, MCP, TBEN and TLBISYNC (input hold)	2.5		2.5		2.5		ns	
11c	$\overline{\text{HRESET}}$ to mode select input hold ($\overline{\text{QACK}}$, $\overline{\text{DRTRY}}$)	0	—	0	—	0	—	ns	2, 4, 5
VM	Measurement Reference Voltage for Inputs	$OV_{DD}/2$						—	—

Notes:
1. Input specifications are measured from the VM of the signal in question to VM of the rising edge of the input SYSCLK. Input and output timings are measured at the pin (see Figure 3-3).
2. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 3-4 on page 23).
3. t_{SYSCLK}, is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a **minimum of 255 bus clocks** after the PLL relock time during the power-on reset sequence.
5. All values are guaranteed by design, and are not tested.

Figure 3-3 provides the input timing diagram for the 750FX.

Figure 3-3. Input Timing Diagram

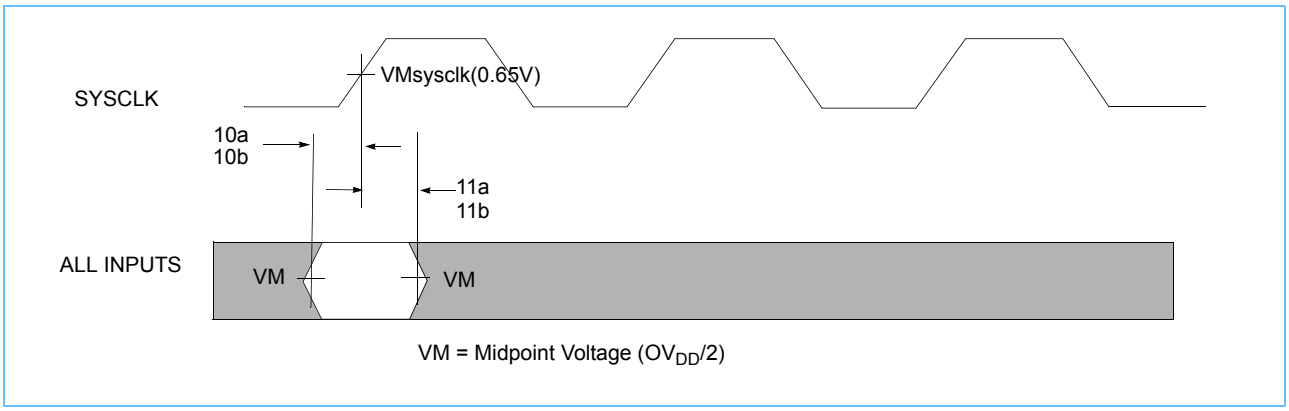
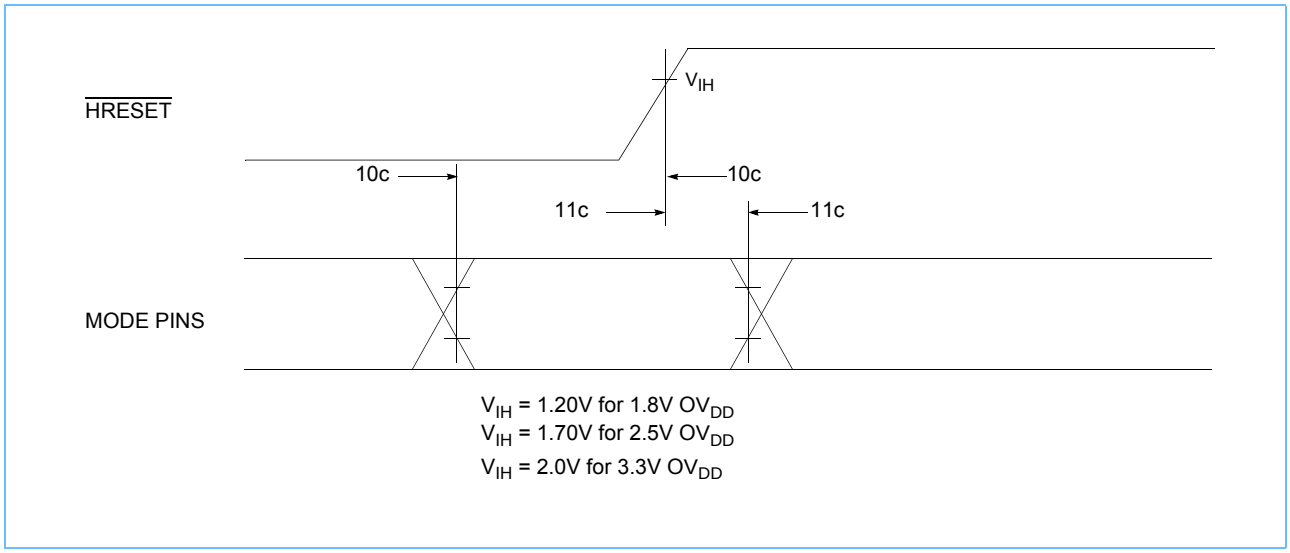


Figure 3-4 provides the mode select input timing diagram for the 750FX.

Figure 3-4. Mode Select Input Timing Diagram



3.6 60x Bus Output AC Specifications

Table 3-8 provides the 60x bus output AC timing specifications for the 750FX as defined in Figure 3-6 on page 26.

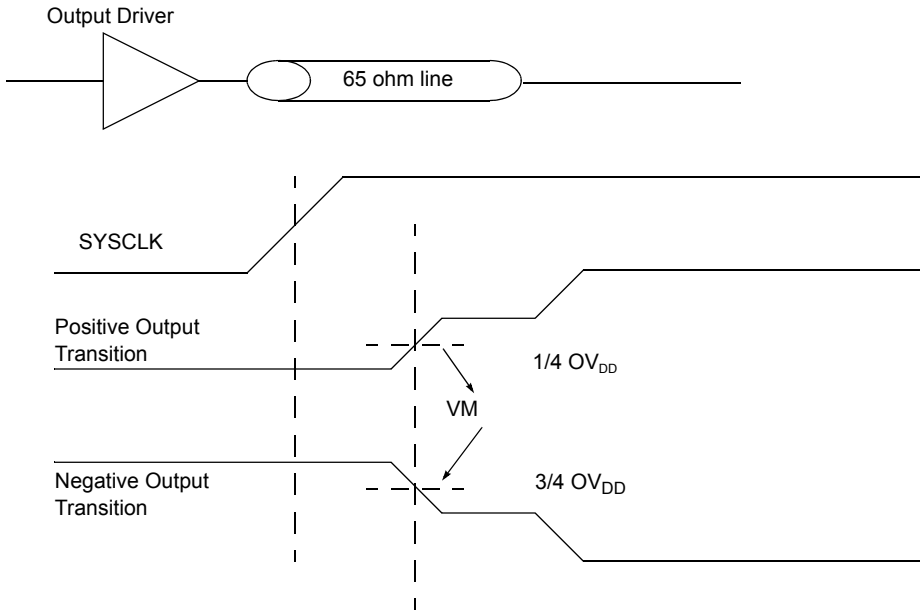
Table 3-8. 60x Bus Output AC Timing Specifications
See *Table 3-2* on page 16 for operating conditions.[1, 5]

Num	Characteristic	1.8V		2.5V		3.3V		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
12	SYSCLK to Output Driven (Output Enable Time)	0.3	–	TBD	–	TBD	–	ns	–
13	SYSCLK to Output Valid	–	2.3	–	2.5	–	2.5	ns	2,6
14	SYSCLK to Output Invalid (Output Hold)	0.6	–	0.3	–	0.3	–	ns	2
15	SYSCLK to Output High Impedance (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$)	–	2.5	–	2.5	–	2.5	ns	–
16	SYSCLK to $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ high impedance after precharge	–	1.0	–	1.0	–	1.0	t_{SYSCLK}	3, 4
17	SYSCLK to $\overline{\text{ARTRY}}$ high impedance before precharge	–	3.0	–	3.0	–	3.0	ns	–
18	SYSCLK to $\overline{\text{ARTRY}}$ precharge enable	0.2× t_{SYSCLK} + 1.0		0.2× t_{SYSCLK} + 1.0	–	0.2× t_{SYSCLK} + 1.0	–	nsi	2, 3, 4
19	Maximum delay to $\overline{\text{ARTRY}}$ precharge	–	1.0	–	1.0	–	1.0	t_{SYSCLK}	3, 4
20	SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge	–	2.0		2.0		2.0	t_{SYSCLK}	3, 4

Notes:

1. All output specifications are measured from the VM of the rising edge of SYSCLK to the output signal level defined in Figure 3-5 on page 25. Both input and output timings are measured at the pin. Timings are determined by design.
2. This minimum parameter assumes CL = 0pF.
3. t_{SYSCLK} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
4. Nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}.
5. Guaranteed by design and characterization, and not tested.
6. Output Valid timing increases as the V_{DD} in reduced. These values assumes V_{DD} minimum of 1.35V.

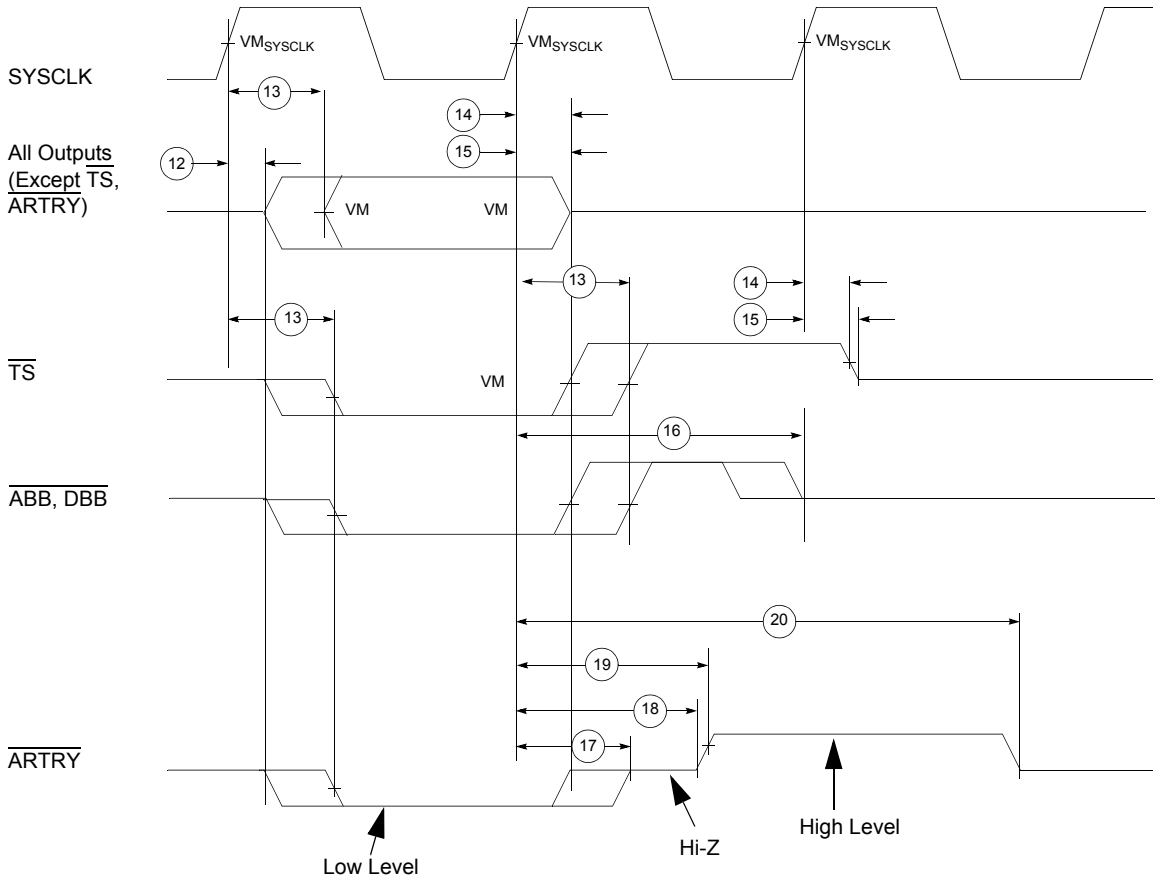
Figure 3-5. Output Valid Timing Definition



Output Transition defined between SYSCLK @ VM and the respective transition level.

Note: The timing definition uses an infinitely long transmission line model.

Figure 3-6. Output Timing Diagram for PowerPC 750FX RISC Microprocessor



Note: SYSCLK VM as defined in *Section 3.3 Clock AC Specifications* on page 19. Output VM as defined in *Section 3-5 Output Valid Timing Definition* on page 25.

3.6.1 IEEE 1149.1 AC Timing Specifications

Table 3-9 on page 27 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in the following figures:

To find out more about...	See...
JTAG Clock Input Timing Diagram figure	Figure 3-7 on page 28
TRST Timing Diagram figure	Figure 3-8 on page 28
Boundary-Scan Timing Diagram figure	Figure 3-9 on page 28
Test Access Port Timing Diagram figure	Figure 3-10 on page 29

The five JTAG signals are; TDI, TDO, TMS, TCK, and $\overline{\text{TRST}}$.

Table 3-9. JTAG AC Timing Specifications (Independent of SYSCLK)
See Table 3-2 on page 16 for operating conditions.

Num	Characteristic	Min.	Max.	Unit	Notes
	TCK frequency of operation	0	25	MHz	
1	TCK cycle time	40	—	ns	
2	TCK clock pulse width measured at 1.1V	15	—	ns	
3	TCK rise and fall times	0	2	ns	4
4	Specification obsolete, intentionally omitted				
5	$\overline{\text{TRST}}$ assert time	25	—	ns	1
6	Boundary-scan input data setup time	0	—	ns	2
7	Boundary-scan input data hold time	13	—	ns	2
8	TCK to output data valid	–	8	ns	3, 5
9	TCK to output high impedance	3	19	ns	3, 4
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	2.5	12	ns	5
13	TCK to TDO high impedance	3	9	ns	4
14	TCK to output data invalid (output hold)	0	–	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. Guaranteed by design.
2. Non-JTAG signal input timing with respect to TCK.
3. Non-JTAG signal output timing with respect to TCK.
4. Guaranteed by characterization and not tested.
5. Minimum specification guaranteed by characterization and not tested.

Figure 3-7 provides the JTAG clock input timing diagram.

Figure 3-7. JTAG Clock Input Timing Diagram

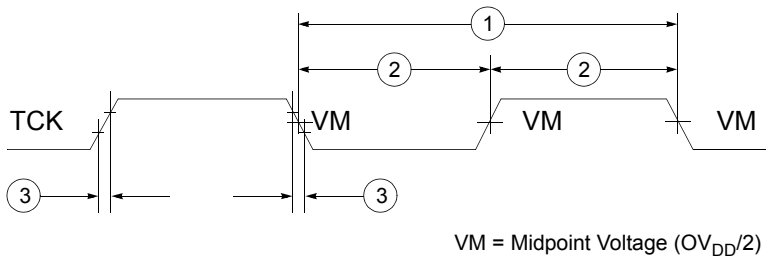


Figure 3-8 provides the $\overline{\text{TRST}}$ timing diagram.

Figure 3-8. $\overline{\text{TRST}}$ Timing Diagram

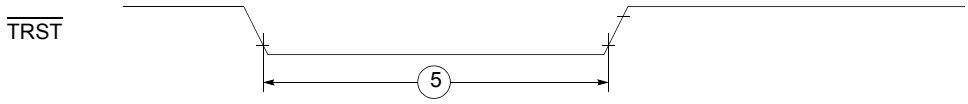


Figure 3-9 provides the boundary-scan timing diagram.

Figure 3-9. Boundary-Scan Timing Diagram

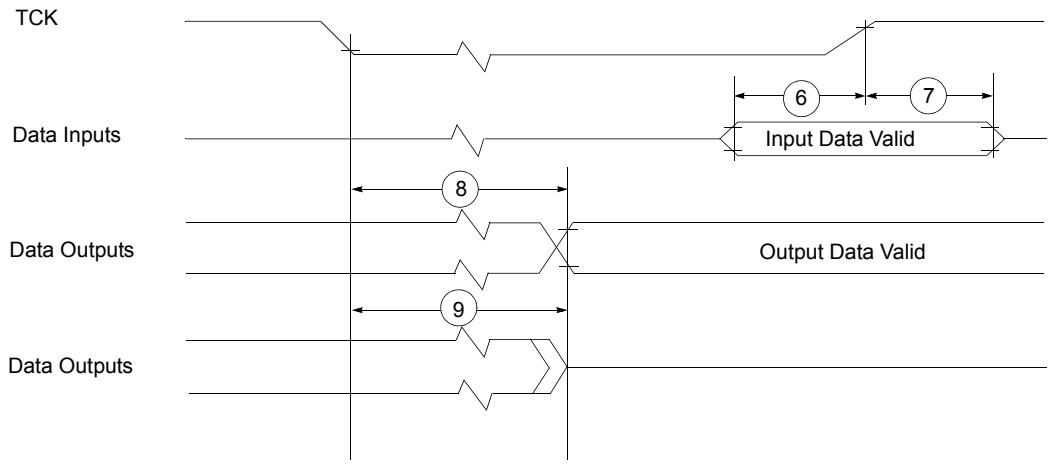
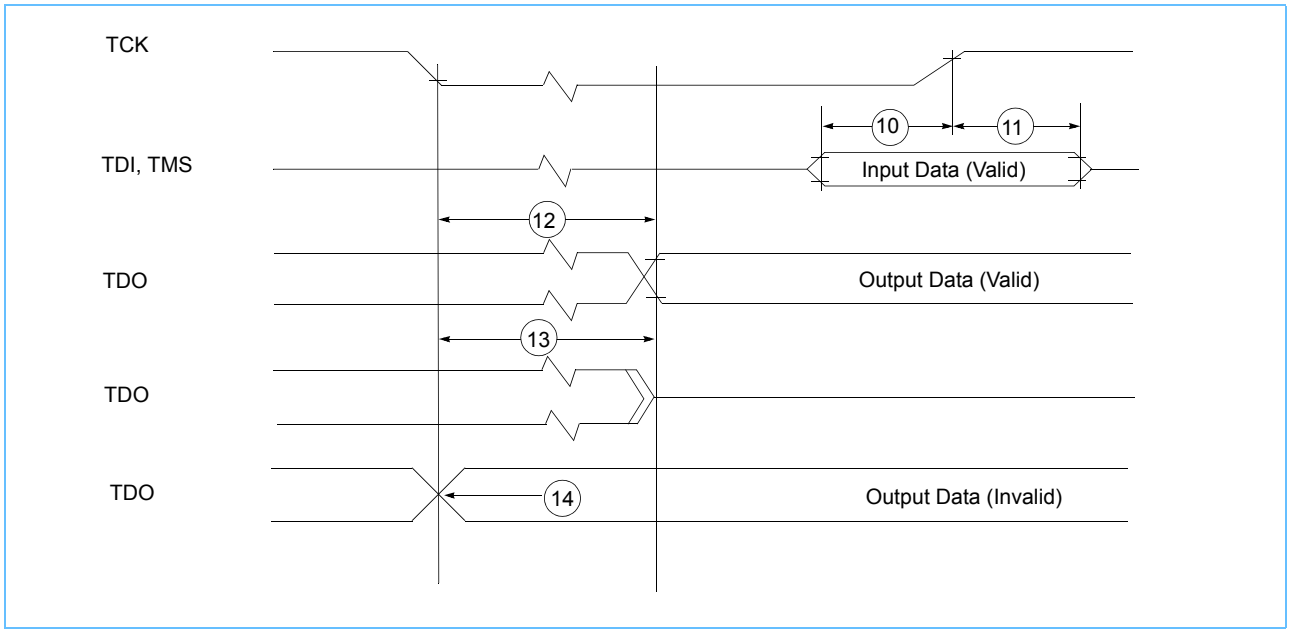


Figure 3-10 provides the test access port timing diagram.

Figure 3-10. Test Access Port Timing Diagram



4. Dimensions and Signal Assignments

IBM offers a ceramic ball grid array (CBGA) which supports 292 balls for the 750FX package.

This section contains several views of the 750FX physical package and descriptions and listings of the signals and ball/pin locations. For more information about the physical layout of the 750FX, see *Table 4-2 Pinout Listing for the CBGA package* on page 33.

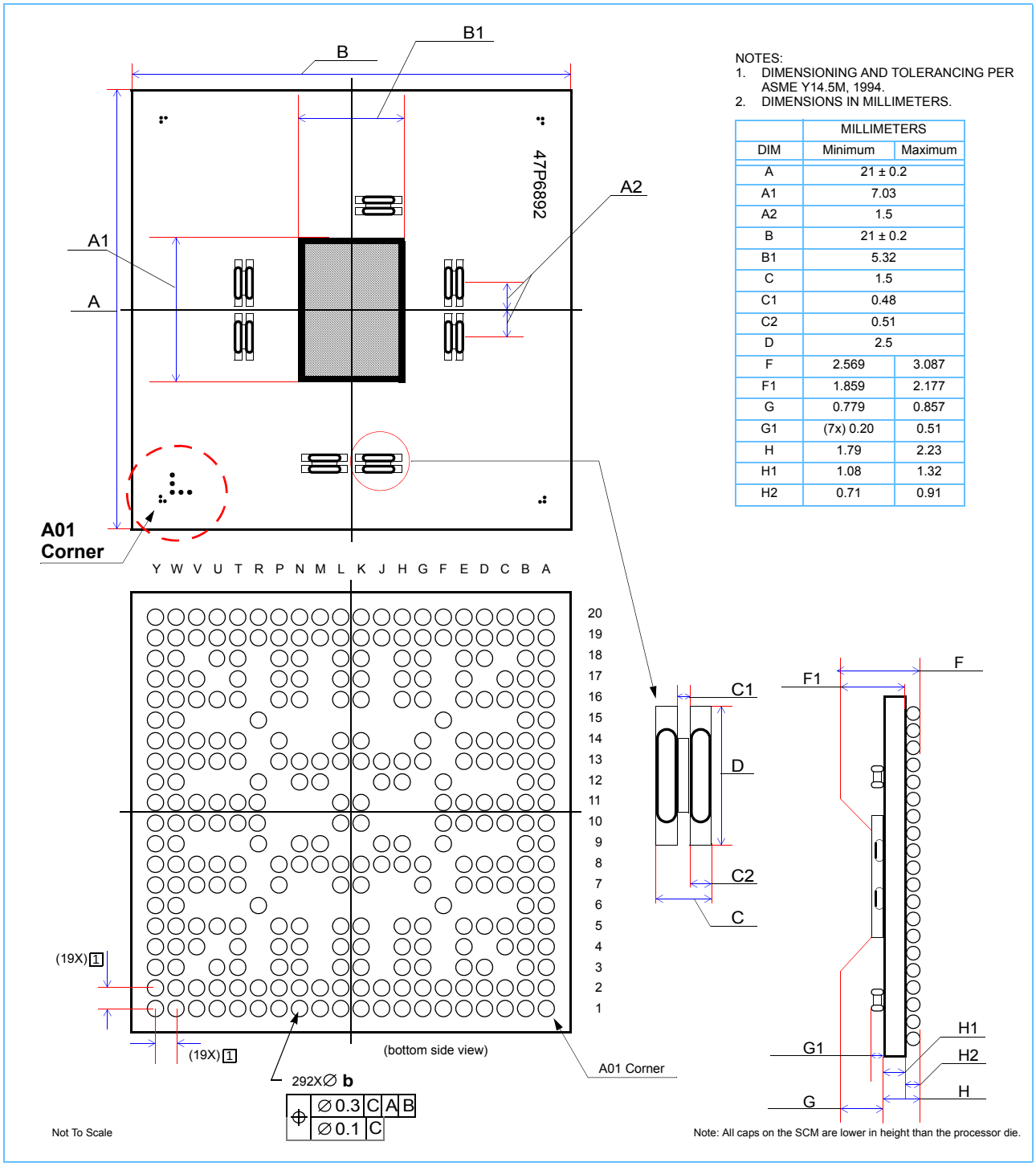
Table 4-1 lists the drawing used in this section and the corresponding IBM drawing number. For the latest package information, obtain the current IBM drawings.

Table 4-1. List of Drawings with IBM Drawing Numbers

For Figure...	See Section...	Package number
Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package figure	*Figure 4-1* on page 31	47P6892
A01 designation for correct placement - Use the 5 plated dots forming a right angle (|_) to properly locate the A01 corner.		

4.1 Package

Figure 4-1. Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.

	MILLIMETERS	
DIM	Minimum	Maximum
A	21 ± 0.2	
A1	7.03	
A2	1.5	
B	21 ± 0.2	
B1	5.32	
C	1.5	
C1	0.48	
C2	0.51	
D	2.5	
F	2.569	3.087
F1	1.859	2.177
G	0.779	0.857
G1	(7x) 0.20	0.51
H	1.79	2.23
H1	1.08	1.32
H2	0.71	0.91

4.2 Microprocessor Ball Placement

Figure 4-2. PowerPC 750FX Microprocessor Ball Placement

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	a6	a8	a3	a2	a0	dh31	dh25	dh26	pd2	dh22	dh19	dh18	dh16	dh15	dh14	dp0	dh9	dh10	dh4	dh2
19	a13	GND	a5	a4	a1	dh29	dp3	dh28	dh23	dh24	dh21	dh20	dp1	dh17	dh11	dh8	dh6	dh5	GND	dh3
18	a11	a10		**OVDD**	GND		**OVDD**	GND		VDD	VDD		GND	**OVDD**		GND	**OVDD**		dh0	pll_cfg0
17	a12	tt1	**OVDD**		a9		dh30	dh27		GND	GND		dh12	dh13		dh1		**OVDD**	pll_cfg1	pll_cfg2
16	a14	a15	GND	ap0	a7		GND	**OVDD**		**OVDD**	**OVDD**		**OVDD**	GND		dh7	pll_cfg3	GND	sysclk	**a2vdd**
15	tt3	ts				VDD									VDD				PLL_RANGE0	**a1vdd**
14	tsiz0	tt2	**OVDD**	tt0	GND		**OVDD**			GND	GND			**OVDD**		GND	PLL_RANGE1	**OVDD**	pll_cfg4	**agnd**
13	ap2	tt4	GND	ap1	VDD		GND	GND	VDD	VDD	VDD	VDD	GND	GND		VDD	llsd_mode	GND	l2_tstclk	l1_tstclk
12	ta	tsiz1				VDD		GND	GND			GND	GND		VDD				mcp	checkstop
11	tbst	tsiz2	VDD	GND	**OVDD**	GND				VDD	VDD				GND	**OVDD**	GND	VDD	tlbisync	hreset
10	dbdis	a16	VDD	GND	**OVDD**	GND				GND	GND				GND	**OVDD**	GND	VDD	smi	ckstp
9	a18	a17				VDD		GND	VDD			VDD	GND		VDD				bvsel	int
8	aack	ap3	GND	a21	VDD		GND	GND	VDD	VDD	VDD	VDD	GND	GND		VDD	qreq	GND	tben	qack
7	a20	a19	**OVDD**	a24	GND		**OVDD**			GND	GND			**OVDD**		GND	dbb	**OVDD**	artry	sreset
6	dbwo	a23				VDD									VDD				tea	abb
5	a22	a26	GND	a25	a31		GND	**OVDD**		**OVDD**	**OVDD**		**OVDD**	GND		clkout	wt	GND	tdo	dbg
4	a28	a27	**OVDD**		dl3		dp5	dl13		GND	GND		dl23	dl26		ci		**OVDD**	bg	rsrv
3	a29	a30		**OVDD**	GND		**OVDD**	GND		VDD	VDD		GND	**OVDD**		GND	**OVDD**		drtry	br
2	dl0	GND	dl2	dl6	dl5	dl11	dl10	dl12	dl16	dl15	dl19	dl20	dl22	dl27	dl28	tck	dl30	tdi	GND	blank
1	dl1	dp4	dl4	dl8	dl7	dl9	dl14	dp6	dl18	dl17	dl21	dp7	dl24	dl25	dl29	dl31	trst	tms	gbl	blank

Note: This view is looking down from above the 750FX placed and soldered on the system board.

4.3 Pinout Listings

Table 4-2 contains the pinout listing for the 750FX CBGA package.

Table 4-2. Pinout Listing for the CBGA package

Signal Name	Pin Number	Active	Input/Output	Notes
A[0:31]	E20, E19, D20, C20, D19, C19, A20, E16, B20, E17, B18, A18, A17, A19, A16, B16, B10, B9, A9, B7, A7, D8, A5, B6, D7, D5, B5, B4, A4, A3, B3, E5.	High	Input/Output	
A1VDD	Y15	—	—	
A2VDD	Y16	—	—	
$\overline{\text{AACK}}$	A8	Low	Input	
$\overline{\text{ABB}}$	Y6	Low	Input/Output	
AGND	Y14	—	—	
AP[0:3]	D16, D13, A13, B8	High	Input/Output	6
$\overline{\text{ARTRY}}$	W7	Low	Input/Output	
$\overline{\text{BG}}$	W4	Low	Input	
BLANK	Y1, Y2	—	—	3
$\overline{\text{BR}}$	Y3	Low	Output	
BVSEL	W9	—	Input	4
$\overline{\text{CHECKSTOP}}$ (CKSTP_OUT)	Y12	Low	Output	
$\overline{\text{CI}}$	T4	Low	Output	
$\overline{\text{CKSTP\_IN}}$	Y10	Low	Input	
CLKOUT	T5	--	Output	
$\overline{\text{DBB}}$	U7	Low	Input/Output	
$\overline{\text{DBDIS}}$	A10	Low	Input	
$\overline{\text{DBG}}$	Y5	Low	Input	
$\overline{\text{DBWO}}$	A6	Low	Input	
DH[0:31]	W18, T17, Y20, Y19, W20, V19, U19, T16, T19, U20, V20, R19, N17, P17, R20, P20, N20, P19, M20, L20, M19, L19, K20, J19, K19, G20, H20, H17, H19, F19, G17, F20	High	Input/Output	
DL[0:31]	A2, A1, C2, E4, C1, E2, D2, E1, D1, F1, G2, F2, H2, H4, G1, K2, J2, K1, J1, L2, M2, L1, N2, N4, N1, P1, P4, P2, R2, R1, U2, T1	High	Input/Output	
DP[0:7]	T20, N19, J20, G19, B1, G4, H1, M1	High	Input/Output	6
$\overline{\text{DRTRY}}$	W3	Low	Input	
$\overline{\text{GBL}}$	W1	Low	Input/Output	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the Input/Output drivers and V_{DD} inputs supply power to the processor core.
3. These pins are reserved for potential future use.
4. BVSEL and L1_TSTCLK select the Input/Output voltage mode on the 60x bus.
5. TCK must be tied high or low for normal machine operation.
6. Address and data parity should be left floating if unused in the design.

Table 4-2. Pinout Listing for the CBGA package (Continued)

Signal Name	Pin Number	Active	Input/Output	Notes
GND	B2, B19, C5, C8, C13, C16, D10, D11, E3, E7, E14, E18, F10, F11, G5, G8, G13, G16, H3, H8, H9, H12, H13, H18, J12, K4, K7, K10, K14, K17, L4, L7, L10, L14, L17, M12, N3, N8, N9, N12, N13, N18, P5, P8. P13, P16, R10, R11, T3, T7, T14, T18, U10, U11, V5, V8, V13,V16, W2, W19,	—	—	
$\overline{\text{HRESET}}$	Y11	Low	Input	
$\overline{\text{INT}}$	Y9	Low	Input	
L1_TSTCLK	Y13	—	Input	4
L2_TSTCLK	W13	See note 1.	Input	1
$\overline{\text{LSSD\_MODE}}$	U13	Low	Input	1
$\overline{\text{MCP}}$	W12	Low	Input	
OV_{DD}	C4, C7, C14, C17, D3, D18, E10, E11, G3, G7, G14, G18, H5, H16, K5, K16, L5, L16, N5, N16, P3, P7, P14, P18, T10, T11, U3, U18, V4, V7, V14, V17	—	—	2
PLL_CFG[0:4]	Y18, W17, Y17, U16, W14	High	Input	
PLL_RANGE[0:1]	W15, U14	High	Input	
$\overline{\text{QACK}}$	Y8	Low	Input	
$\overline{\text{QREQ}}$	U8	Low	Output	
$\overline{\text{RSRV}}$	Y4	Low	Output	
$\overline{\text{SMI}}$	W10	Low	Input	
$\overline{\text{SRESET}}$	Y7	Low	Input	
SYSCLK	W16	—	Input	
$\overline{\text{TA}}$	A12	Low	Input	
TBEN	W8	High	Input	
$\overline{\text{TBST}}$	A11	Low	Input/Output	
TCK	T2	High	Input	5
TDI	V2	High	Input	
TDO	W5	High	Output	
$\overline{\text{TEA}}$	W6	Low	Input	
$\overline{\text{TLBISYNC}}$	W11	Low	Input	
TMS	V1	High	Input	
$\overline{\text{TRST}}$	U1	Low	Input	
$\overline{\text{TS}}$	B15	Low	Input/Output	
TSIZ[0:2]	A14, B12, B11	High	Output	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the Input/Output drivers and V_{DD} inputs supply power to the processor core.
3. These pins are reserved for potential future use.
4. BVSEL and L1_TSTCLK select the Input/Output voltage mode on the 60x bus.
5. TCK must be tied high or low for normal machine operation.
6. Address and data parity should be left floating if unused in the design.

Table 4-2. Pinout Listing for the CBGA package (Continued)

Signal Name	Pin Number	Active	Input/Output	Notes
TT[0:4]	D14, B17, B14, A15, B13	High	Input/Output	
V_{DD}	C10, C11, E8, E13, F6, F9, F12, F15, J8, J9, J13, K3, K8, K11, K13, K18, L3, L8, L11, L13, L18, M8, M9, M13, R6, R9, R12, R15, T8, T13, V10, V11	—	—	2
$\overline{WT}$	U5	Low	Output	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the Input/Output drivers and V_{DD} inputs supply power to the processor core.
3. These pins are reserved for potential future use.
4. BVSEL and L1_TSTCLK select the Input/Output voltage mode on the 60x bus.
5. TCK must be tied high or low for normal machine operation.
6. Address and data parity should be left floating if unused in the design.

Table 4-3. Signal Listing for the CBGA Package

Signal Name	Pin Count	Active	Input/Output	Notes
A[0:31]	32	High	Input/Output	
A1VDD	1			Supply for PLL0
A2VDD	1			Supply for PLL1
$\overline{\text{AACK}}$	1	Low	Input	
$\overline{\text{ABB}}$	1	Low	Input/Output	
AGND	1			Ground for PLL
AP[0:3]	4	High	Input/Output	
$\overline{\text{ARTRY}}$	1	Low	Input/Output	
$\overline{\text{BG}}$	1	Low	Input	
$\overline{\text{BR}}$	1	Low	Output	
BVSEL	1	High	Input	I/O voltage mode select for 60x bus. See section 5.9.3 for setup conditions
$\overline{\text{CI}}$	1	Low	Output	
$\overline{\text{CKSTP\_IN}}$	1	Low	Input	
CKSTP_OUT	1	Low	Output	
CLKOUT	1		Output	
$\overline{\text{DBB}}$	1	Low	Input/Output	
$\overline{\text{DBDIS}}$	1	Low	Input	
$\overline{\text{DBG}}$	1	Low	Input	
DBWO	1	Low	Input	
DH[0:31]	32	High	Input/Output	
DL[0:31]	32	High	Input/Output	
DP[0:31]	8	High	Input/Output	
$\overline{\text{DRTRY}}$	1	Low	Input	
$\overline{\text{GBL}}$	1	Low	Input/Output	
Ground	60			Common Ground
$\overline{\text{HRESET}}$	1	Low	Input	
$\overline{\text{INT}}$	1	Low	Input	
L1_TSTCLK	1	High	Input	I/O voltage mode select for 60x bus. See section 5.9.3 for setup conditions
L2_TSTCLK	1	High	Input	These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
$\overline{\text{LSSD\_MODE}}$	1	Low	Input	These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
$\overline{\text{MCP}}$	1	Low	Input	
OV_{DD}	32			Supply for Receiver/Drivers
PLL_CFG[0:4]	5	High	Input	

Table 4-3. Signal Listing for the CBGA Package (Continued)

Signal Name	Pin Count	Active	Input/Output	Notes
PLL_RANGE[0:1]	2	High	Input	
$\overline{\text{QACK}}$	1	Low	Input	
$\overline{\text{QREQ}}$	1	Low	Output	
$\overline{\text{RSRV}}$	1	Low	Output	
$\overline{\text{SMI}}$	1	Low	Input	
$\overline{\text{SRESET}}$	1	Low	Input	
SYSCLK	1	—	Input	
$\overline{\text{TA}}$	1	Low	Input	
TBEN	1	High	Input	
$\overline{\text{TBST}}$	1	Low	Input/Output	
TCK	1	High	Input	
TDI	1	High	Input	
TDO	1	High	Output	
$\overline{\text{TEA}}$	1	Low	Input	
$\overline{\text{TLBISYNC}}$	1	Low	Input	OPTIONAL: 64/32-Bit Data Bus mode select. This function will be set when $\overline{\text{HRESET}}$ transitions (low to high). $\overline{\text{TLBISYNC}}$: high = 64-bit mode, low =32-bit mode.
TMS	1	High	Input	
$\overline{\text{TRST}}$	1	Low	Input	
$\overline{\text{TS}}$	1	Low	Input/Output	
TSIZ[0:2]	3	High	Output	
TT[0:4]	5	High	Input/Output	
V_{DD}	32			Supply for Core
$\overline{\text{WT}}$	1	Low	Output	

Table 4-4. Signal Locations

Signal	Ball Location	Signal	Ball Location	Signal	Ball Location	Signal	Ball Location
A0	E20	DH0	W18	DL0	A2	$\overline{\text{AACK}}$	A8
A1	E19	DH1	T17	DL1	A1	$\overline{\text{ABB}}$	Y6
A2	D20	DH2	Y20	DL2	C2	AGND	Y14
A3	C20	DH3	Y19	DL3	E4	$\overline{\text{ARTRY}}$	W7
A4	D19	DH4	W20	DL4	C1	$\overline{\text{BG}}$	W4
A5	C19	DH5	V19	DL5	E2	$\overline{\text{BR}}$	Y3
A6	A20	DH6	U19	DL6	D2	BVSEL	W9
A7	E16	DH7	T16	DL7	E1	$\overline{\text{CHECKSTOP}}$ ($\overline{\text{CKSTP\_OUT}}$)	Y12
A8	B20	DH8	T19	DL8	D1	$\overline{\text{CI}}$	T4
A9	E17	DH9	U20	DL9	F1	$\overline{\text{CKSTP}}$ ($\overline{\text{CKSTP\_IN}}$)	Y10
A10	B18	DH10	V20	DL10	G2	$\overline{\text{DBB}}$	U7
A11	A18	DH11	R19	DL11	F2	$\overline{\text{DBDIS}}$	A10
A12	A17	DH12	N17	DL12	H2	$\overline{\text{DBG}}$	Y5
A13	A19	DH13	P17	DL13	H4	$\overline{\text{DBWO}}$	A6
A14	A16	DH14	R20	DL14	G1	$\overline{\text{DRTRY}}$	W3
A15	B16	DH15	P20	DL15	K2	$\overline{\text{GBL}}$	W1
A16	B10	DH16	N20	DL16	J2	$\overline{\text{HRESET}}$	Y11
A17	B9	DH17	P19	DL17	K1	$\overline{\text{INT}}$	Y9
A18	A9	DH18	M20	DL18	J1	L1_TSTCLK	Y13
A19	B7	DH19	L20	DL19	L2	L2_TSTCLK	W13
A20	A7	DH20	M19	DL20	M2	$\overline{\text{LSSD\_MODE}}$	U13
A21	D8	DH21	L19	DL21	L1	$\overline{\text{MCP}}$	W12
A22	A5	DH22	K20	DL22	N2	PLL_CFG0	Y18
A23	B6	DH23	J19	DL23	N4	PLL_CFG1	W17
A24	D7	DH24	K19	DL24	N1	PLL_CFG2	Y17
A25	D5	DH25	G20	DL25	P1	PLL_CFG3	U16
A26	B5	DH26	H20	DL26	P4	PLL_CFG4	W14
A27	B4	DH27	H17	DL27	P2	PLL_RANGE0	W15
A28	A4	DH28	H19	DL28	R2	PLL_RANGE1	U14
A29	A3	DH29	F19	DL29	R1	$\overline{\text{QACK}}$	Y8
A30	B3	DH30	G17	DL30	U2	$\overline{\text{QREQ}}$	U8
A31	E5	DH31	F20	DL31	T1	$\overline{\text{RSRV}}$	Y4
						$\overline{\text{SMI}}$	W10
						$\overline{\text{SRESET}}$	Y7
						SYSCLK	W16
						$\overline{\text{TA}}$	A12

Table 4-4. Signal Locations (Continued)

Signal	Ball Location	Signal	Ball Location	Signal	Ball Location	Signal	Ball Location
		AP0	D16	DP0	T20	TBEN	W8
		AP1	D13	DP1	N19	$\overline{\text{TBST}}$	A11
		AP2	A13	DP2	J20	TCK	T2
		AP3	B8	DP3	G19	TDI	V2
				DP4	B1	TDO	W5
				DP5	G4	$\overline{\text{TEA}}$	W6
				DP6	H1	$\overline{\text{TLBISYNC}}$	W11
				DP7	M1	TMS	V1
						$\overline{\text{TRST}}$	U1
						$\overline{\text{TS}}$	B15
						TSIZ0	A14
						TSIZ1	B12
						TSIZ2	B11
						TT0	D14
						TT1	B17
						TT2	B14
						TT3	A15
						TT4	B13
						$\overline{\text{WT}}$	U5

Table 4-5. Voltage and Ground Assignments

$A1v_{DD}$	$A2v_{DD}$	Ov_{DD}	Ov_{DD}	V_{DD}	V_{DD}	GND	GND
Y15	Y16	C4	C7	C10	C11	B2	B19
		C14	C17	E8	E13	C5	C8
		D3	D18	F6	F9	C13	C16
		E10	E11	F12	F15	D10	D11
		G3	G7	J8	J9	E3	E7
		G14	G18	J13	K3	E14	E18
		H5	H16	K8	K11	F10	F11
		K5	K16	K13	K18	G5	G8
		L5	L16	L3	L8	G13	G16
		N5	N16	L11	L13	H3	H8
		P3	P7	L18	M8	H9	H12
		P14	P18	M9	M13	H13	H18
		T10	T11	R6	R9	J12	K4
		U3	U18	R12	R15	K7	K10
		V4	V7	T8	T13	K14	K17
		V14	V17	V10	V11	L4	L7
						L10	L14
						L17	M12
						N3	N8
						N9	N12
						N13	N18
						P5	P8
						P13	P16
						R10	R11
						T3	T7
						T14	T18
						U10	U11
						V5	V8
						V13	V16
						W2	W19

5. System Design Information

This section provides electrical and thermal design recommendations for successful application of the 750FX.

5.1 Core Voltage Operation

The 750FX supports a single V_{DD} setting for a specific application condition. The AV_{DD} supplie(s) can be set to the same voltage as V_{DD}, and the PLL_RANGE[0:1] bits **must** be set to 00 for applications of 600 MHz or above frequencies. Applications requiring lower speeds and core voltages, should refer to the *IBM 750FX Datasheet Supplement for DD2.X Product Revisions,* which provides more detailed information of these application conditions.

5.2 Low Voltage Operation at Lower Frequency

Due to the relationship of power to frequency and voltage (power proportional to frequency and square of voltage), running the processor at an associated lower voltage and lower frequency results in significant power savings. Low voltage application conditions are noted in the *IBM 750FX Datasheet Supplement for DD2.X Product Revisions.*

After the 750FX application condition, within the supported limits, has been selected, the 750FX's dual PLL feature can also be used to provide additional power savings.

5.2.1 Overview

The 750FX design includes two PLLs (PLL0 and PLL1), allowing the processor clock frequency to dynamically change between the PLL frequencies via software control. Use the bits in the HID1 register to specify:

1. The frequency range of each PLL
2. The clock multiplier for each PLL
3. External or internal control of PLL0
4. A bit to choose which PLL is selected (which is the source of the processor clock at any given time)

Note: The PLL configuration must adhere to the maximum allowed frequency as specified in the *IBM 750FX Datasheet Supplement for DD2.X Product Revisions*, for the minimum V_{DD} condition. Voltages (V_{DD}/AV_{DD}) should remain constant at all times.

At power-on reset, the HID1 register contains zeroes for all the non-read-only bits (bits 7 to 31). This configuration corresponds to the selection of PLL0 as the source of the processor clocks and selects the external configuration and range pins to control PLL0. The external configuration and range pin values are accessible to software using HID1 read-only bits 0-6. PLL1 is always controlled by its internal configuration and range bits. The HID1 setting associated with hard reset corresponds to a PLL1 configuration of clock off, and selection of the medium frequency range.

As stated in the hardware specification, HRESET must be asserted during power up long enough for the PLL(s) to lock, and for the internal hardware to be reset. Once this timing is satisfied, HRESET can be negated. The processor now will proceed to execute instructions, clocked by PLL0 as configured via the external pins. The processor clock frequency can be modified from this initial setting in one of two ways. First, as with earlier designs, HRESET can be asserted, and the external configuration pins can be set to a new

value. The machine state is lost in this process, and, as always, HRESET must be held asserted while the PLL relocks, and the internal state is reset. Second, the introduction of another PLL provides an alternative means of changing the processor clock frequency, which does not involve the loss of machine state, nor a delay for PLL relock.

The following sequence can be used to change processor clock frequency.

Note: Assume PLL0 is currently the source for the processor clock.

1. Configure PLL1 to produce the desired clock frequency, by setting HID1[PR1] and HID1[PC1] to the appropriate values.
2. Wait for PLL1 to lock. The lock time is the same for both PLLs and is provided in the hardware specification.
3. Set HID1[PS] to 1 to initiate the transition from PLL0 to PLL1 as the source of the processor clocks. From the time the HID1 register is updated to select the new PLL, the transition to the new clock frequency will complete within three (3) bus cycles. After the transition, the HID(PSS) bit indicates which PLL is in use.

   After both PLLs are running and locked, the processor frequency can be toggled with very low latency. For example, when it is time to change back to the PLL0 frequency, there is no need to wait for PLL lock. HID1[PS] can be reset to 0, causing the processor clock source to transition from PLL1 back to PLL0. If PLL0 will not be needed for some time, it can be configured to be off while not in use. This is done by resetting the HID1[PC0] field to 0, and setting HID1[PI0] to 1. Turning the non-selected PLL off results in a modest power savings, but introduces added latency when changing frequency. If PLL0 is configured to be off, the procedure for switching to PLL0 as the selected PLL involves changing the configuration and range bits, waiting for lock, and then selecting PLL0, as described in the previous paragraph.

5.2.2 Restrictions and Considerations for PLL Configuration

Avoid the following when reconfiguring the PLLs:

1. The configuration and range bits in HID1 should only be modified for the non-selected PLL, since it will require time to lock before it can be used as the source for the processor clock.
2. The HID1[PI0] bit should only be modified when PLL0 is not selected.
3. Whenever one of the PLLs is reconfigured, it must not be selected as the active PLL until enough time has elapsed for the PLL to lock.
4. At all times, the frequency of the processor clock, as determined by the various configuration settings, must be within the specification range for the current operating conditions.
5. Never select a PLL that is in the ‘off’ configuration.

Configuration Restriction on Frequency Transitions

It is considered a programming error to switch from one PLL to the other when both are configured in a *half-cycle* multiplier mode. For example, with PLL0 configured in 9:2 mode (cfg = 01001) and PLL1 configured in 13:2 mode (cfg = 01101), changing the select bit (HID1[PS]) is not allowed. In cases where such a pairing of configurations is desired, an intermediate full-cycle configuration must be used between the two half-cycle modes. For example, with PLL0 at 9:2, PLL1, configured at 6:1 is selected, then PLL0 is reconfigured at 13:2, locked and selected.

5.2.3 PLL Range[0:1] Definitions for Dual PLL Operation

The dual PLLs on the 750FX are configured by the PLL_CFG[0:4] and PLL_Range[0:1] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL range configuration, for dual PLL operation, for the 750FX is shown in the following table.

Table 5-1. PLL Range [0:1] Definitions for Dual PLL Operation

PLL_RANGE[0:1]	PLL Frequency Range
00	600-733 MHz
10	Below 600 MHz
01	Reserved
11	Reserved

5.2.4 PLL Configuration

The PLL configuration for the 750FX is shown in the following table for nominal frequencies.

Table 5-2. 750FX Microprocessor PLL Configuration

PLL_CFG [0:4]		Processor to Bus Frequency Ratio (PTBFR)	Frequency Range Supported by VCO having an example range of...			
			SYSCLK[6] (in MHz)		Core (in MHz)	
bin	dec		Min. ($SYSCLK_{MIN}$)	Max. ($SYSCLK_{MAX}$)	Min. ($Core\ Frequency_{MIN}$)	Max. ($Core\ Frequency_{MAX}$)
00000	0	OFF	N/A	N/A	Off	Off
00001	1	OFF	N/A	N/A	Off	Off
00010	2	PLL Bypass[3]	N/A	N/A	N/A	N/A
00011	3	PLL Bypass[3]	N/A	N/A	N/A	N/A
00100	4	2x[1]	-	-	-	-
00101	5	2.5x[1]	-	-	-	-
00110	6	3x[1]	-	-	-	-
00111	7	3.5x	114	150[5]	400	525
01000	8	4x	100	150	400	600
01001	9	4.5x	89	150	400	675
01010	10	5x	80	147	400	733
01011	11	5.5x	73	133	400	733
01100	12	6x	67	122	400	733
01101	13	6.5x	62	113	400	733
01110	14	7x	57	105	400	733
01111	15	7.5x	53	98	400	733
10000	16	8x	50	92	400	733
10001	17	8.5x	47	86	400	733
10010	18	9x	44	81	400	733
10011	19	9.5x	42	77	400	733
10100	20	10x	40	73	400	733
10101	21	11x	36[2]	66	400	733
10110	22	12x	33[2]	61	400	733

Notes:

1. The 2X- 3X Processor to Bus Ratios are currently not supported.
2. SYSCLK minimum is limited by the lowest frequency that manufacturing will support, see Table 3-6, “Clock AC Timing Specifications” on page 19 for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. In Clock-off mode, no clocking occurs inside the 750FX regardless of the SYSCLK input.
5. The SYSCLK limit is 150MHz, as specified in Table 3-6 on page 19. Applications requiring SYSCLK over 150MHz must be investigated by application conditions.
6. SYSCLK = CoreFrequency/PBFR
   The SYSCLK frequency equals the core frequency divided by the processor-to-bus frequency ratio (PBFR).

Table 5-2. 750FX Microprocessor PLL Configuration (Continued)

PLL_CFG [0:4]		Processor to Bus Frequency Ratio (PTBFR)	Frequency Range Supported by VCO having an example range of...			
			SYSCLK[6] (in MHz)		Core (in MHz)	
bin	dec		Min. ($SYSCLK_{MIN}$)	Max. ($SYSCLK_{MAX}$)	Min. ($Core\ Frequency_{MIN}$)	Max. ($Core\ Frequency_{MAX}$)
10111	23	13x	31[2]	56	400	733
11000	24	14x	29[2]	53	400	733
11001	25	15x	27[2]	49	400	733
11010	26	16x	25[2]	46	400	733
11011	27	17x	24[2]	43	400	733
11100	28	18x	22[2]	40.1	400	733
11101	29	19x	21[2]	36	400	733
11110	30	20x	20[2]	37	400	733
11111	31	Off[4]	N/A	N/A	N/A	N/A

Notes:

1. The 2X- 3X Processor to Bus Ratios are currently not supported.
2. SYSCLK minimum is limited by the lowest frequency that manufacturing will support, see Table 3-6, “Clock AC Timing Specifications” on page 19 for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. In Clock-off mode, no clocking occurs inside the 750FX regardless of the SYSCLK input.
5. The SYSCLK limit is 150MHz, as specified in Table 3-6 on page 19. Applications requiring SYSCLK over 150MHz must be investigated by application conditions.
6. SYSCLK = CoreFrequency/PBFR
   The SYSCLK frequency equals the core frequency divided by the processor-to-bus frequency ratio (PBFR).

5.3 PLL Power Supply Filtering

The 750FX microprocessor has two separate AV_{DD} signals (A1VDD and A2VDD) which provide power to the clock generation phase-locked loop.

Most designs are expected to utilize a single PLL configuration mode throughout the application. These type of designs should use the default, A1VDD (PLL0) and tie the A2VDD signal to ground (GND) through a 100 ohm resistor. This is shown in Figure 5-1 on page 47

For designs planning to optimize power savings through dynamic switching between these dual PLL circuits, it is recommended, though not required, that each AV_{DD} have a separate voltage input and filter circuit. This optional circuit is included in.

To ensure stability of the internal clock, the power supplied to the AV_{DD} input signals should be filtered using a circuit similar to the one shown in Figure 5-1 on page 47. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible.

For descriptions of the sample PLL power supply filtering circuits, see *Table 5-3*.

Table 5-3. Sample PLL Power Supply Filtering Circuits

Samples of PLL Power Supply Filtering Circuits					
Circuit Description	Number of Filtering Circuits	Ferrite Beads	Circuit Figure	Recommended Circuit Design	Notes
Single PLL circuit configuration that uses the A1VDD and ties the A2VDD pin to GND.	1	1	*Figure 5-1* on page 47	Yes	1, 2
Single PLL circuit configuration that uses both the A1VDD and the A2VDD pins and a single ferrite bead	1	1	*Figure 5-2* on page 48	Optional	1, 2
Dual PLL configuration that uses a separate circuit for the A1VDD pin and for the A2VDD the pin.	2	2	*Figure 5-3* on page 49	Yes	2, 3

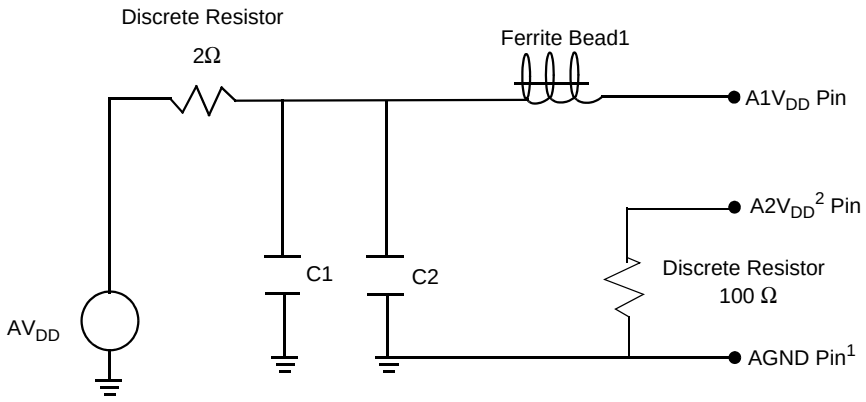
Notes:

1. Optional configurations are supported, though not recommended.
2. This circuit design can be used with the Dual PLL feature enabled, though optimum power savings may not be realized. For additional information, see *Figure 5-3 Dual PLL Power Supply Filter Circuits* on page 49.
3. This circuit design can be used with the Dual PLL feature enabled to optimize power savings.

Figure 5-1. Single PLL Power Supply Filter Circuit with $A1V_{DD}$ Pin and $A2V_{DD}$ Pin Tied to GND

Single PLL ($A1V_{DD}$) Power Supply Filter Circuit

(Recommended)



Legend:

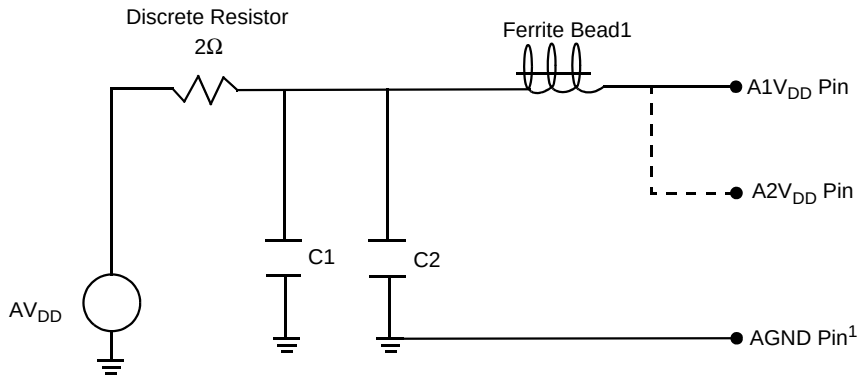
Item	Description/Value
Resistor	2Ω , 100Ω
C1	0.1 µF, Ceramic
C2	10.0 µF, Ceramic
Ferrite Bead	Murata BLM21P300S or similar

Note:
1. Connected to ground without a filter.
2. Single PLL0 only

Figure 5-2. PLL Power Supply Filter Circuit with Two AV_{DD} Pins and One Ferrite

Single PLL (AV_{DD}) Power Supply Filter Circuit

(Optional)



Legend:

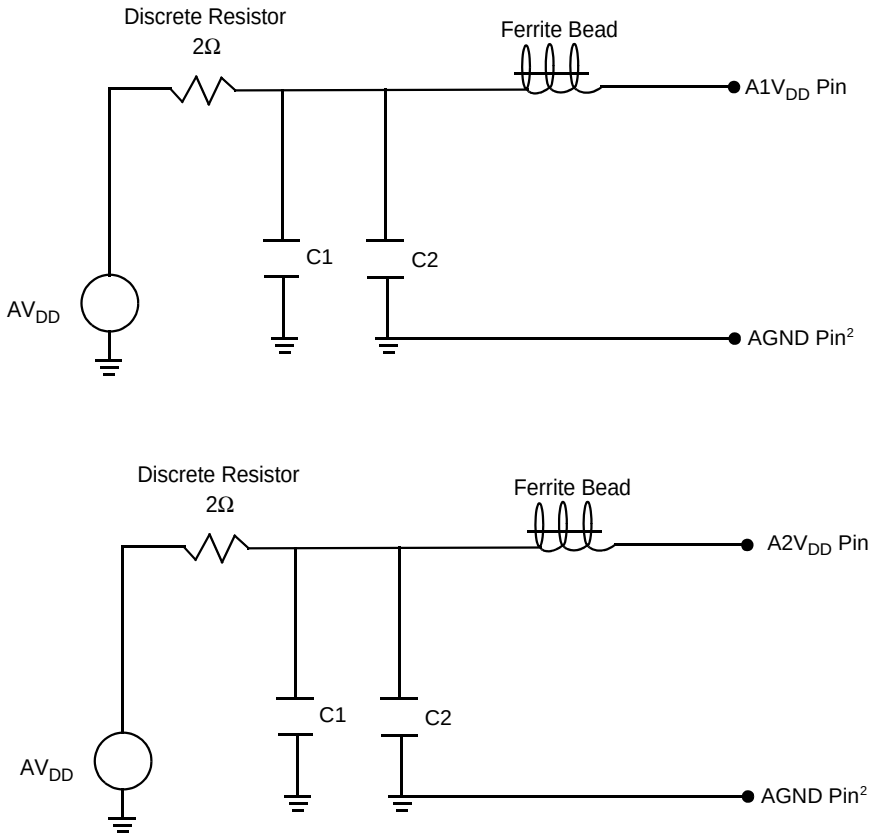
Item	Description/Value
Resistor	2Ω
C1	0.1 µF Ceramic
C2	10.0 µF Ceramic
Ferrite Bead	Murata BLM21P300S or similar

Note:
1. Connected to ground without a filter.

Figure 5-3. Dual PLL Power Supply Filter Circuits

Dual PLL (AV_{DD}) Power Supply Filter Circuits[1]

(Recommended configuration if Dual PLL feature is enabled.)



Item	Description/Value
Resistor	2Ω
C1	0.1 µF Ceramic
C2	10.0 µF Ceramic
Ferrite Bead	Murata BLM21P300S or similar

Notes:

1. The dual PLL power supply circuits shown in this figure are recommended for a design that uses the Dual PLL feature. For more information about the Dual PLL feature, see Section 5.2 “Low Voltage Operation at Lower Frequency,” on page 41.
2. Connected to ground without a filter.

5.4 Decoupling Recommendations

Capacitor decoupling is required for the 750FX. Decoupling capacitors act to reduce high frequency chip switching noise and provide localized bulk charge storage to reduce major power surge effects. Guidelines for high frequency noise decoupling will be provided. Bulk decoupling requires a more complete understanding of the system and system power architecture which precludes discussion in this document.

High frequency decoupling capacitors should be located as close as possible to the processor with low lead inductance to the ground and voltage planes.

Decoupling capacitors are recommended on the back of the card, directly opposite the module. The recommended placement and number of decoupling capacitors, 34 V_{DD}-Gnd caps and 44 OV_{DD}-GND caps are described in Figure 5-4, Orientation and Layout of the 750FX Decoupling Capacitors. The recommended decoupling capacitor specifications are provided in *Table 5-4 Recommended Decoupling Capacitor Specifications* on page 50. The placement and usage described here are guidelines for decoupling capacitors and should be applied for System designs.

Table 5-4. Recommended Decoupling Capacitor Specifications

Item	Description
Decoupling Capacitor Specifications	Type X5R or Y5V 10 V minimum 0402 size 40 x 20 mils, nominally 1.0 mm x 0.5 mm ± 0.1 mm on both dimensions
	100 nF
Recommended minimum number of decoupling capacitors on the back of the card:	34 V_{DD}-GND caps 44 OV_{DD}-GND caps

Note: The decoupling capacitor electrodes are located directly opposite from their corresponding BGA pins where possible. Also, each electrode for each decoupling capacitor needs to be connected to one or more BGA pins (balls) with a short electrical path. Thus, through-vias adjacent to the decoupling capacitors are recommended.

The card designer can expand on the decoupling capacitor recommendations by doing the following:

- Adding additional decoupling capacitors
  If using additional decoupling capacitors, verify that these additional capacitors do not reduce the number of card vias or cause the vias to lose proximity to each capacitor electrode.
- Adding additional through-vias or blind-vias
  Card technologies are available that will reduce the inductance between the decoupling capacitor and the BGA pin (ball). Replacing single vias with multiple vias is certainly approved. Place GND vias close to V_{DD} or OV_{DD} vias to reduce loop inductance.

Figure 5-4. Orientation and Layout of the 750FX Decoupling Capacitors

Note: Figure 5-4 shows the recommended decoupling capacitor positions under application conditions. In test mode, pins C11 and G8 can be used as kelvin probes, in which case the pins should be disconnected from card gnd and vdd. Capacitors should not be connected to the pins during kelvin probe voltage measurement.

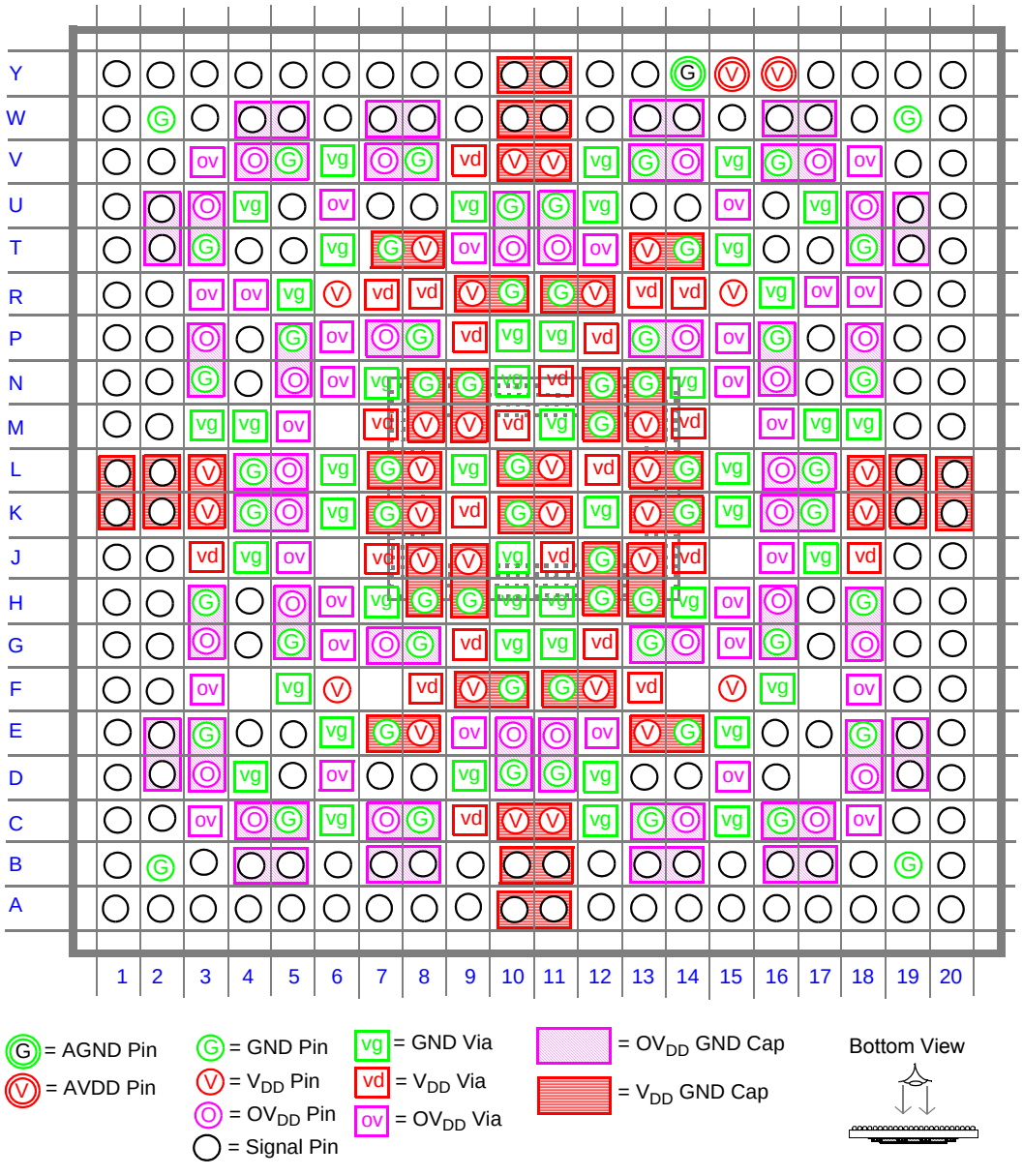
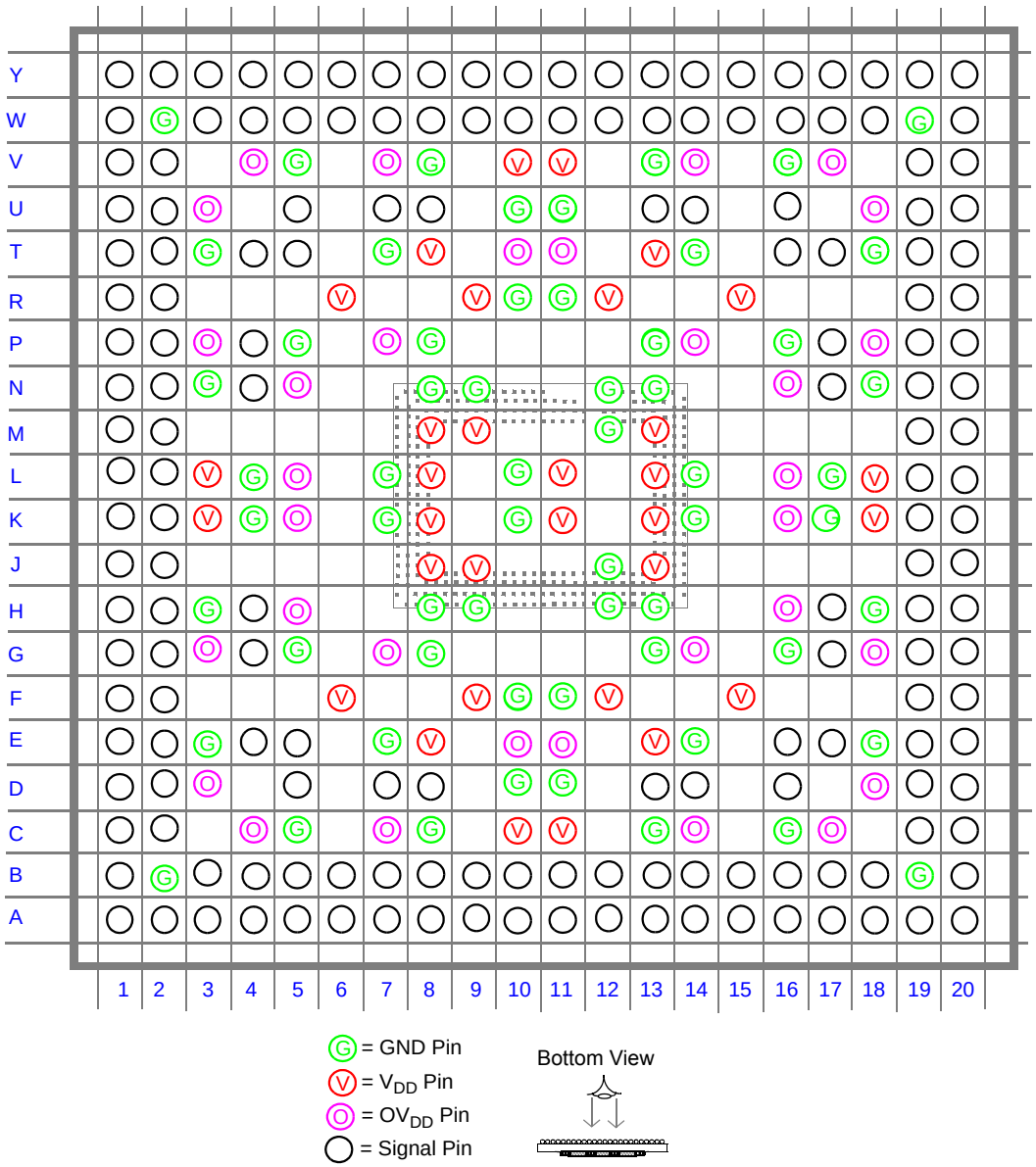


Figure 5-5. 750FX Pin Locations: OV_{DD}, V_{DD}, GND, and Signal Pins

Note: Figure 5-5 shows the recommended decoupling capacitor positions under application conditions. In test mode, pins C11 and G8 can be used as kelvin probes, in which case the pins should be disconnected from card gnd and vdd. Capacitors should not be connected to the pins during kelvin probe voltage measurement.



5.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, AV_{DD} and GND pins of the 750FX.

5.6 Output Buffer DC Impedance

The 750FX 60x drivers were characterized over various process, voltage, and temperature conditions. To measure Z_0, an external resistor is connected to the chip pad, either to OV_{DD} or GND. Then the value of such resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 5-6).

The output impedance is actually the average of two resistances: the resistance of the pull-up and the resistance of pull-down devices. When Data is held low, SW1 is closed (SW2 is open), and R_N is trimmed until Pad = $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW2 is closed (SW1 is open), and R_P is trimmed until Pad = $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. With a properly designed driver R_P and R_N are close to each other in value, then $Z_0 = (R_P + R_N)/2$.

Figure 5-6. Driver Impedance Measurement

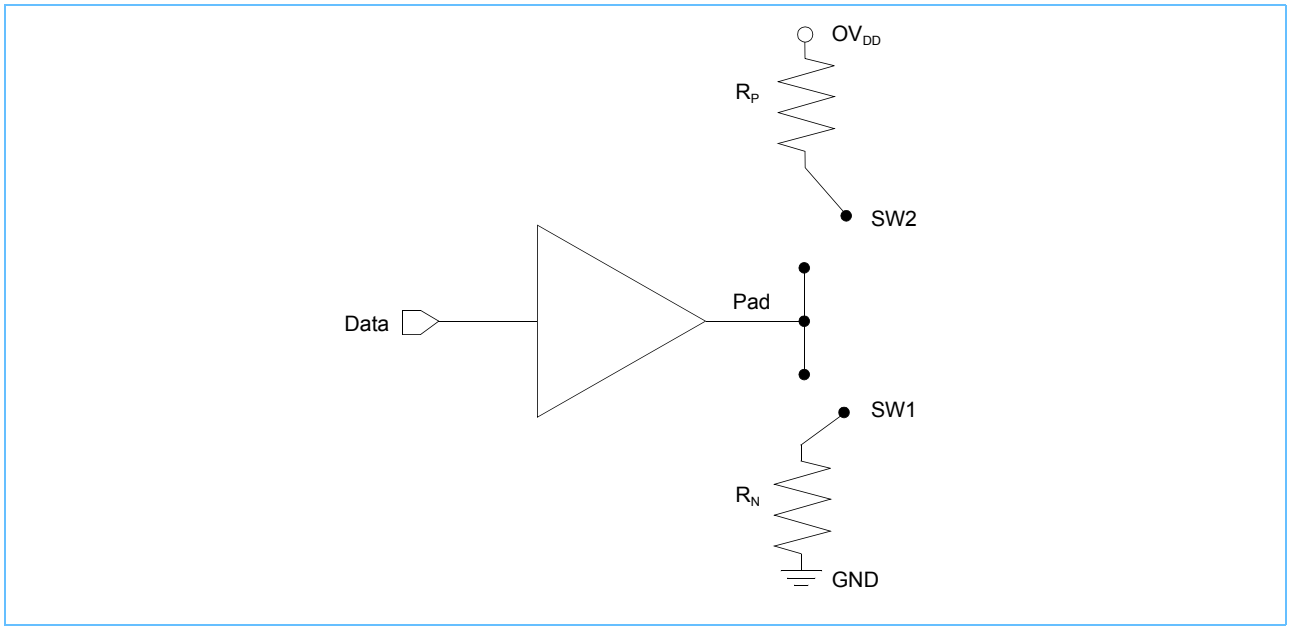


Table 5-5 summarizes the driver impedance characteristics a designer uses to design a typical process.

Table 5-5. Driver Impedance Characteristics

Process	60x Impedance (Ω)	OV_{DD} (V)	Temperature (°C)
Worst	50	1.70	105
Typical	44	1.80	85
Best	36	1.90	0
Worst	50	238	105
Typical	44	2.50	85
Best	36	2.63	0
Worst	65	3.14	105
Typical	50	3.30	85
Best	35	3.46	0

5.6.1 Input-Output Usage

Table 5-6 Input-Output Usage on page 55 provides details on the input-output usage of the PowerPC 750FX RISC Microprocessor signals. The *Usage Group* column refers to the general functional category of the signal.

In the PowerPC 750FX RISC Microprocessor, certain input-output signals have pullups and pulldowns, which may or may not be enabled. In *Table 5-6 Input-Output Usage* on page 55, the *Input/Output with Internal Resistors* column defines which signals have these pullups or pulldowns, and their active or inactive state. The *Level Protect* column defines which signals have the designated function added to their Input/Output cell. For more about Level Protection, see *Section 5.9.1 Level Protection* on page 66.

Caution: This section is based on preliminary information and is subject to change.

Table 5-6. Input-Output Usage

750FX Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
A1VDD	—	—	Power Supply					
A2VDD	—	—	Power Supply					
A[0:31]	N/A	Input/Output	Address Bus		Keeper			1, 3, 4
AACK	Low	Input	Address Termination		Keeper		must be actively driven	3, 4, 5
$\overline{\text{ABB}}$	Low	Input/Output			Keeper	5K Ω	pullup required to OV_{DD}	3, 4, 5
AGND	—	—	Power Supply					
AP[0:3]	High	Input/Output			Keeper			3, 4
$\overline{\text{ARTRY}}$	Low	Input/Output	Address Termination		Keeper	5K Ω	pullup required to OV_{DD}	3, 4, 5
$\overline{\text{BG}}$	Low	Input	Address Arbitration		Keeper		active driver or pulldown	3, 4, 5
$\overline{\text{BR}}$	Low	Output	Address Arbitration		Keeper		chip actively drives	3, 4, 5
BVSEL	N/A	Input	Input/Output Level			5K Ω	pullup/pulldown, as required	5
$\overline{\text{CHECKSTOP}}$	Low	Output	Interrupt/Resets		Keeper	5K Ω	pullup required to OV_{DD}	3, 4, 5
$\overline{\text{CI}}$	Low	Output	Transfer Attributes		Keeper			1, 3, 4
$\overline{\text{CKSTP\_IN}}$	Low	Input	Interrupt/Resets		Keeper		must be actively driven	3, 4, 5
CLKOUT	Low	Output			Keeper			3, 4
$\overline{\text{DBB}}$	Low	Input/Output			Keeper	5K Ω	pullup required to OV_{DD}	3, 4, 5
$\overline{\text{DBDIS}}$	Low	Input			Keeper			3, 4
$\overline{\text{DBG}}$	Low	Input	Data Arbitration		Keeper		active driver or tie low	3, 4, 5
$\overline{\text{DBWO}}$	Low	Input			Keeper			3, 4

Notes:

1. Depends on the system design. The electrical characteristics of the 750FX do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{TRST}}$ are signals used for ESP and RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and PowerPC 750FX RISC Microprocessor. (Refer to Figure 5-7 on page 59.)
3. Keepers prevent floating nets from entering the forbidden zone and causing a slight amount of additional current flow in the input circuits.
4. If other components on 60x bus call for a signal to maintain a particular level while it is not being actively driven, then an external resistor (or whatever) must be used. Do not count on the keepers.
5. The 750FX does not require external pullups on address and data lines. Control lines must be treated individually.

Table 5-6. Input-Output Usage (Continued)

750FX Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
DH[0:31]	N/A	Input/Output	Data Bus		Keeper			1, 3, 4
DL[0:31]	N/A	Input/Output	Data Bus		Keeper			1, 3, 4
DP[0:7]	High	Input/Output						
$\overline{\text{DRTRY}}$	Low	Input			Keeper			3, 4
$\overline{\text{GBL}}$	Low	Input/Output	Transfer Attributes		Keeper			1, 3, 4
GND	—	—	Power Supply					
$\overline{\text{HRESET}}$	Low	Input	Interrupt/Resets		Keeper		active driver	2, 3, 4, 5
$\overline{\text{INT}}$	Low	Input	Interrupt/Resets		Keeper		active driver or pullup	3, 4, 5
L1_TSTCLK	Low	Input	LSSD	Not enabled		5K Ω	pullup/pulldown, as required	5
L2_TSTCLK	Low	Input	LSSD	Not enabled		5K Ω	pullup required to OV_{DD}	5
$\overline{\text{LSSD\_MODE}}$	Low	Input	LSSD	Not enabled		5K Ω	pullup required to OV_{DD}	5
$\overline{\text{MCP}}$	Low	Input	Interrupt/Resets		Keeper		active driver or pullup	3, 4, 5
OV_{DD}	—	—	Power Supply					
PLL_CFG[0:4]	N/A	Input	Clock Control		Keeper	As required	pullup/pulldown, as required	3, 4, 5
PLL_RANGE[0:1]	N/A	Input			Keeper	As required	pullup/pulldown, as required	3, 4, 5
$\overline{\text{QACK}}$	Low	Input	Control		Keeper		must be actively driven	3, 4, 5
$\overline{\text{QREQ}}$	Low	Out	Status/Control		Keeper		chip actively drives	3, 4, 5
$\overline{\text{RSRV}}$	Low	Out			Keeper		no connect	3, 4, 5
$\overline{\text{SMI}}$	Low	Input			Keeper			3, 4
$\overline{\text{SRESET}}$	Low	Input	Interrupt/Resets		Keeper		active driver or pullup	2, 3, 4, 5

Notes:

1. Depends on the system design. The electrical characteristics of the 750FX do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{TRST}}$ are signals used for ESP and RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and PowerPC 750FX RISC Microprocessor. (Refer to Figure 5-7 on page 59.)
3. Keepers prevent floating nets from entering the forbidden zone and causing a slight amount of additional current flow in the input circuits.
4. If other components on 60x bus call for a signal to maintain a particular level while it is not being actively driven, then an external resistor (or whatever) must be used. Do not count on the keepers.
5. The 750FX does not require external pullups on address and data lines. Control lines must be treated individually.

Table 5-6. Input-Output Usage (Continued)

750FX Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
SYSCLK	Low	Input	Clock Control		Keeper	No resistor by design	active driver	3, 4, 5
$\overline{TA}$	Low	Input	Data Termination		Keeper		active driver	3, 4, 5
TBEN	High	Input						
$\overline{TBST}$	Low	Input/Output	Transfer Attributes		Keeper			1, 3, 4
TCK	High	Input	JTAG	Not enabled		External pulldown	5K Ω to GND	5
TDI	High	Input	JTAG	Enabled high	Internal enabled		50µa@2.5V 25µa@1.8V (the pullup current for the internal resistor)	5
TDO	High	Out	JTAG		Keeper			3, 4
$\overline{TEA}$	Low	Input	Data Termination		Keeper		active driver or pullup	3, 4, 5
$\overline{TLBISYNC}$	Low	Input	Control		Keeper		must be actively driven	3, 4
TMS	High	Input	JTAG	Enabled high	Internal enabled		50µa@2.5V 25µa@1.8V (the pullup current for the internal resistor)	5
$\overline{TRST}$	Low	Input	JTAG	Enabled high	Internal enabled		50µa@2.5V 25µa@1.8V (the pullup current for the internal resistor)	2, 5
$\overline{TS}$	Low	Input/Output	Address Start		Keeper	5K Ω	pullup required to OV_{DD}	3, 4, 5
TSIZ[0:2]	N/A	Out	Transfer Attributes		Keeper			1, 3, 4

Notes:

1. Depends on the system design. The electrical characteristics of the 750FX do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. $\overline{HRESET}$, $\overline{SRESET}$, and $\overline{TRST}$ are signals used for ESP and RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and PowerPC 750FX RISC Microprocessor. (Refer to Figure 5-7 on page 59.)
3. Keepers prevent floating nets from entering the forbidden zone and causing a slight amount of additional current flow in the input circuits.
4. If other components on 60x bus call for a signal to maintain a particular level while it is not being actively driven, then an external resistor (or whatever) must be used. Do not count on the keepers.
5. The 750FX does not require external pullups on address and data lines. Control lines must be treated individually.

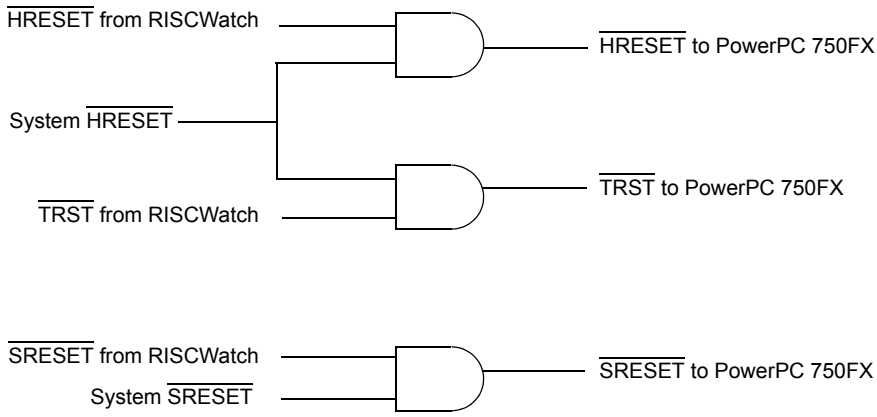
Table 5-6. Input-Output Usage (Continued)

750FX Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
TT[0:4]	N/A	Input/Output	Transfer Attributes		Keeper			1, 3, 4
V_{DD}	—	—	Power Supply					
$\overline{WT}$	Low	Out	Transfer Attributes		Keeper			1, 3, 4

Notes:

1. Depends on the system design. The electrical characteristics of the 750FX do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. $\overline{HRESET}$, $\overline{SRESET}$, and $\overline{TRST}$ are signals used for ESP and RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and PowerPC 750FX RISC Microprocessor. (Refer to Figure 5-7 on page 59.)
3. Keepers prevent floating nets from entering the forbidden zone and causing a slight amount of additional current flow in the input circuits.
4. If other components on 60x bus call for a signal to maintain a particular level while it is not being actively driven, then an external resistor (or whatever) must be used. Do not count on the keepers.
5. The 750FX does not require external pullups on address and data lines. Control lines must be treated individually.

Figure 5-7. IBM RISCWatch™ JTAG to HRESET, TRST, and SRESET Signal Connector



Note: See notes for Table 5-6, “Input-Output Usage” on page 55.

5.7 Thermal Management Information

This section provides thermal management information for the CBGA package for air cooled applications. Proper thermal control design is primarily dependent upon the system-level design; that is, the heat sink, air flow, and the thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, mounting clip, or a screw assembly, see *Figure 5-8 Package Exploded Cross-Sectional View with Several Heat Sink Options* on page 60.

Note: This section is based on preliminary information and is subject to change.

Figure 5-8. Package Exploded Cross-Sectional View with Several Heat Sink Options

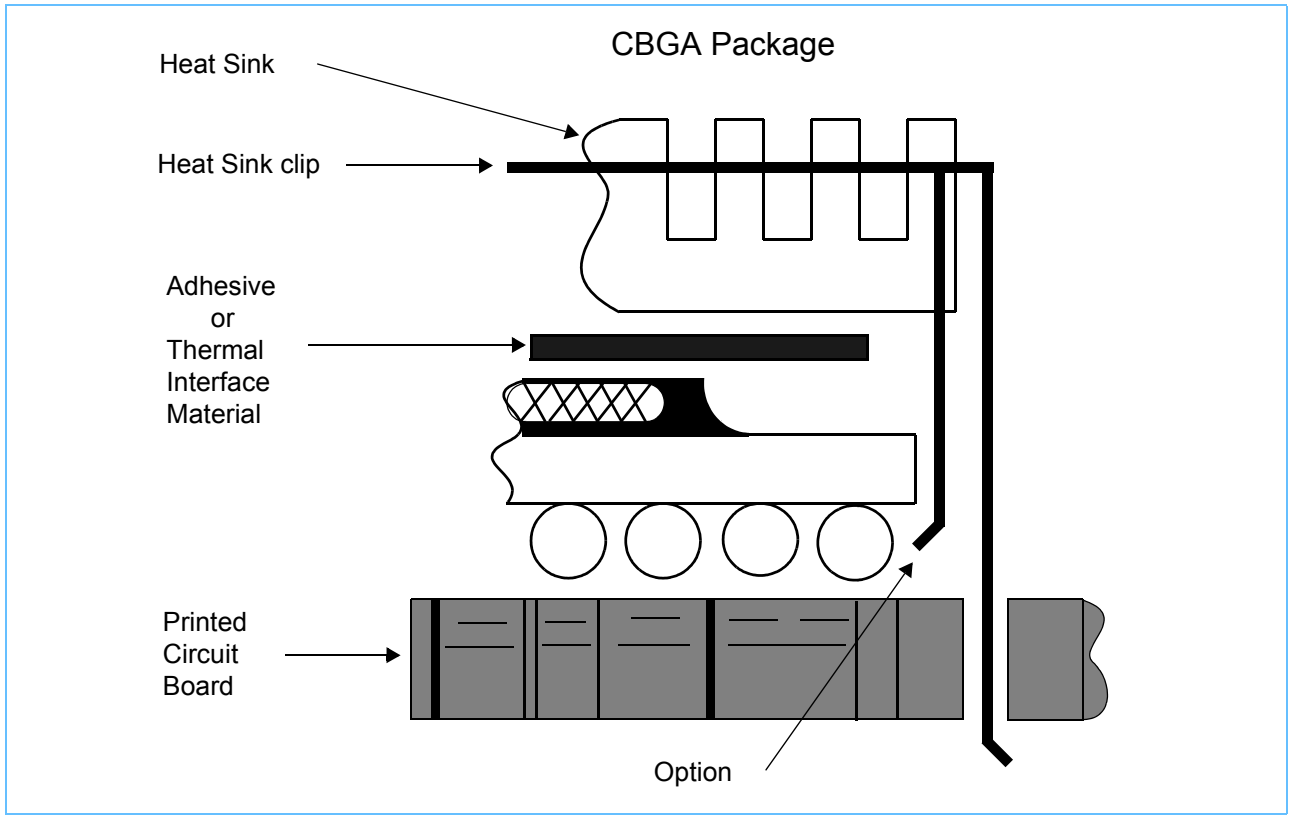


Table 5-7. Maximum Heatsink Weight Limit for the CBGA

Force	Maximum
Maximum dynamic compressive force allowed on the BGA balls	42.9 N
Maximum dynamic tensile force allowed on the BGA balls	9.05 N
Maximum dynamic compressive force allowed on the chip	14.8 N
Maximum mass of module + heatsink when heatsink is not bolted to card	70g

The board designer can choose between several types of heat sinks to place on the 750FX. There are several commercially-available heat sinks for the 750FX provided by the vendors listed in Table 5-8 on page 61.

Table 5-8. 750FX Heat Sink Vendors

Company Names and Addresses for Heat Sink Vendors
Chip Coolers, Inc. 333 Strawberry Field Rd. Warwick, RI 02887-6979 401-739-7600 800-227-0254 (USA/Canada) http://www.chipcoolers.com
Thermalloy 2021 W. Valley View Lane P.O. Box 810839 Dallas, TX 75731 214-243-4321 http://www.aavidthermalloy.com
International Electronic Research Corporation (IERC) 135 W. Magnolia Blvd. Burbank, CA 91502 818-842-7277 http://www.ctscorp.com/ierc
Aavid Engineering One Kool Path Laconic, NH 03247-0440 603-528-3400 http://www.aavid.com
Wakefield Engineering 60 Audubon Rd. Wakefield, MA 01880 617-245-5900 http://www.wakefield.com

5.7.1 Thermal Assist Unit

The thermal sensor in the Thermal Assist Unit (TAU) has not been characterized to determine the basic uncalibrated accuracy. The relationship between the actual junction temperature and the temperature indicated by THRM1 and THRM2 is not well known.

IBM recommends that the TAU in these devices be calibrated before use. Calibration methods are discussed in the IBM Application Note ***Calibrating the Thermal Assist Unit in the IBM25PPC750L Processors***. Although this note was written for the 750L, the calibration methods discussed in this document also apply to the 750FX.

IBM is planning to perform the characterization work necessary to establish the performance of the TAU. The results of this work are not expected to eliminate the calibration requirement, but will allow designers to make a more informed choice of calibration methods.

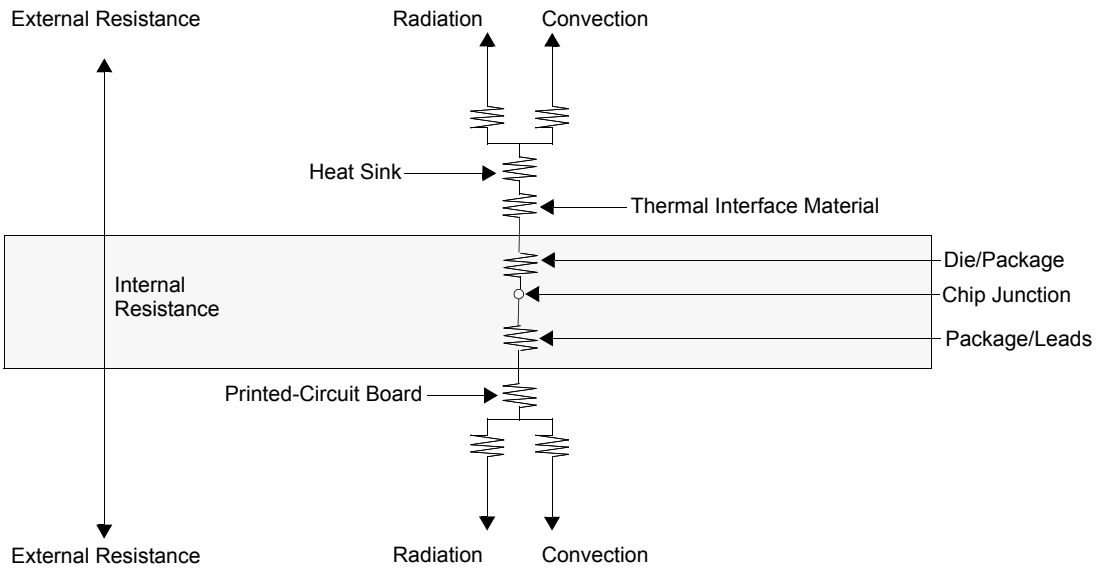
5.7.2 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 3-3 on page 16, the intrinsic conduction thermal resistance paths are as follows.

- Die junction-to-case thermal resistance (Primary thermal path)
- Die junction-to-lead thermal resistance (Not normally a significant thermal path)
- Die junction-to-ambient thermal resistance (Largely dependent on customer-supplied heatsink)

Figure 5-9 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 5-9. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



(Note the internal versus external package resistance.)

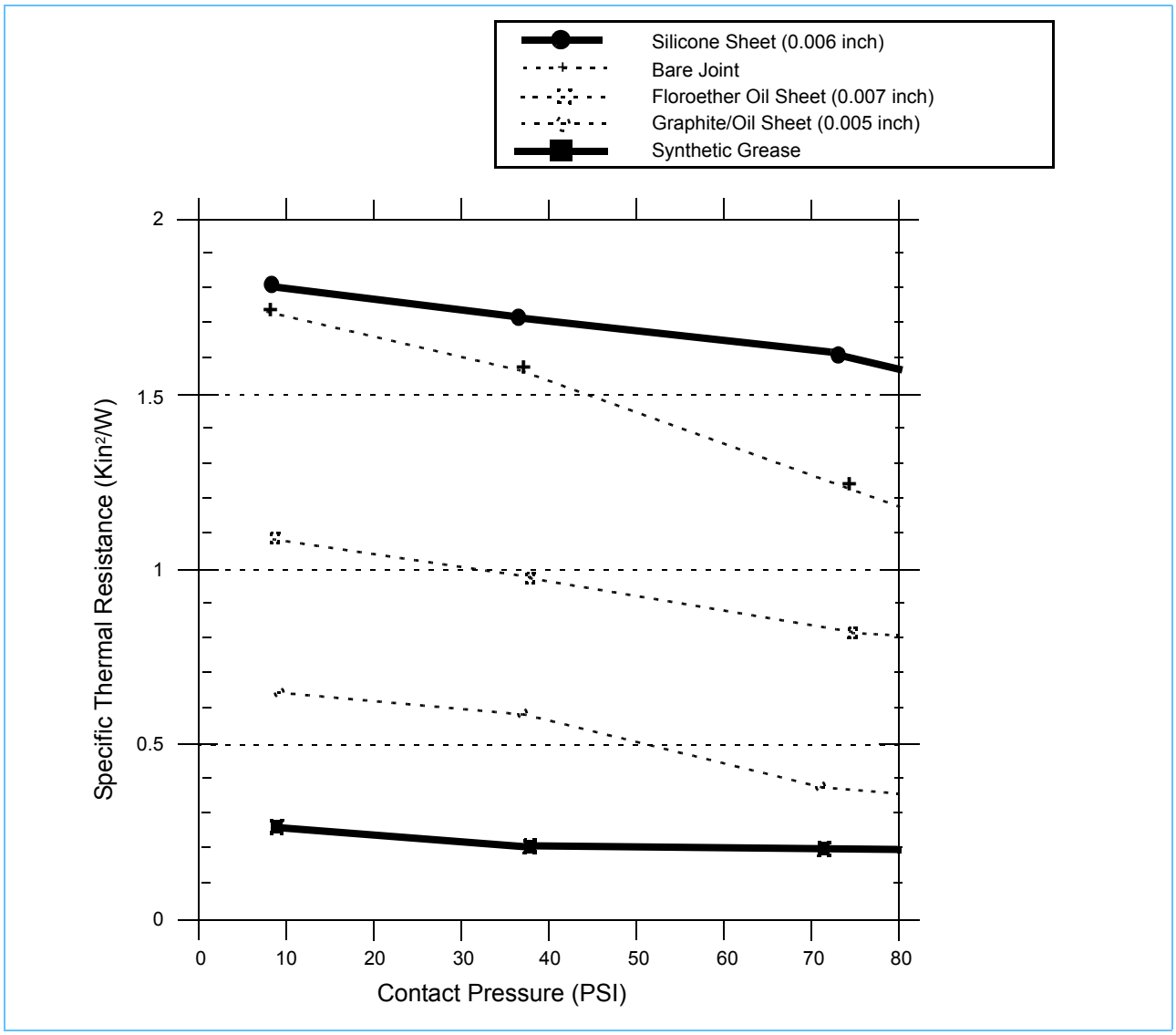
Heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink; where it is removed by forced-air convection. Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

5.7.3 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by a spring clip mechanism, Figure 5-10 shows the thermal performance of three thin-sheet thermal-interface materials (silicon, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease, as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 5-8). Therefore the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors – thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so forth.

Figure 5-10. Thermal Performance of Select Thermal Interface Material



The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Table 5-9. 750FX Thermal Interface and Adhesive Materials Vendors

Company Names and Addresses for Thermal Interfaces and Adhesive Materials Vendors
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 0997 Midland, MI 48686-0997 517-496-4000
Chomerics, Inc. 77 Dragon Court Woburn, MA 01888-4850 617-935-4850
Thermagon, Inc. 3256 West 25th Street Cleveland, OH 44109-1668 216-741-7659
Loctite Corporation 1001 Trout Brook Crossing Rocky Hill, CT 06067 860-571-5100
AI Technology 1425 Lower Ferry Road Trent, NJ 08618 609-882-2332

Section 5.8 on page 64 provides a heat sink selection example using one of the commercially available heat sinks.

5.8 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows.

$$T_J = T_A + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

Where:

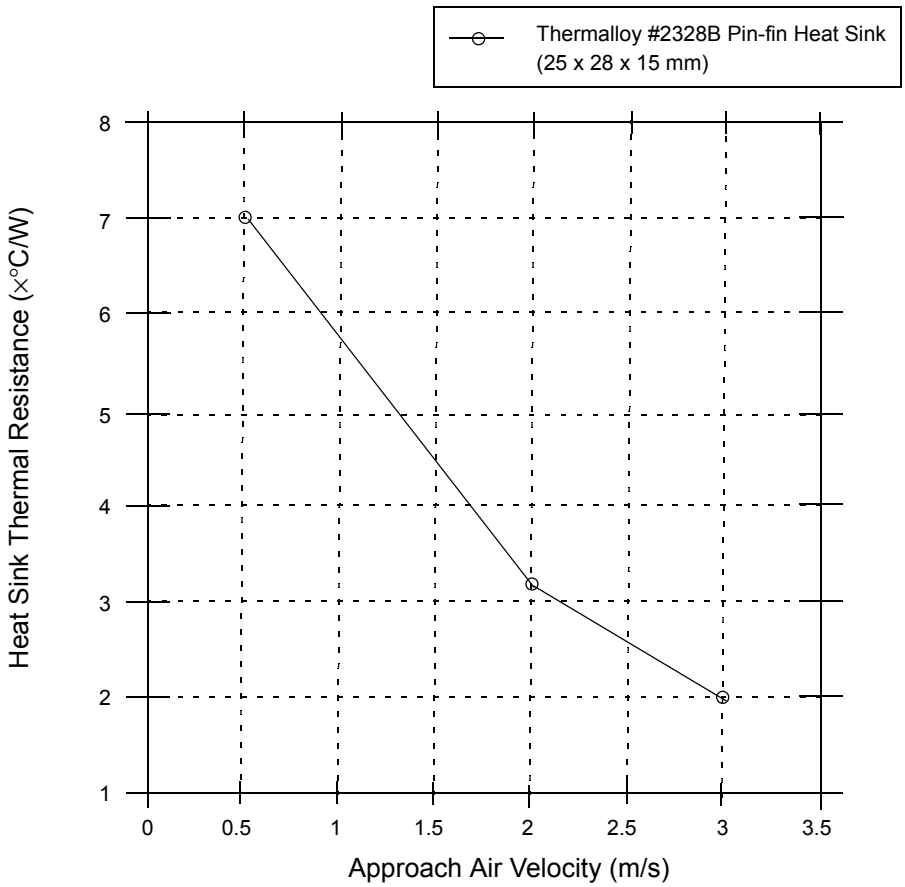
T_J is the die-junction temperature
T_A is the inlet cabinet ambient temperature
T_R is the air temperature rise within the system cabinet
θ_{JC} is the junction-to-case thermal resistance
θ_{INT} is the thermal resistance of the thermal interface material
θ_{SA} is the heat sink-to-ambient thermal resistance
P_D is the power dissipated by the device

Typical die-junction temperatures (T_J) should be maintained less than the value specified in Table 3-3 on page 16. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the computer cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30 to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5 to 10°C. The thermal resistance of the interface material (θ_{INT}) is typically about 1°C/W. Assuming a T_A of 30°C, a T_R of 5°C, a CBGA package θ_{JC} = 0.03, and a power dissipation (P_D) of 5.0 watts, the following expression for T_J is obtained.

Die-junction temperature: $T_J = 30°C + 5°C + (0.03°C/W + 1.0°C/W + \theta_{SA}) \times 5W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{SA}) versus air flow velocity is shown in Figure 5-11.

Figure 5-11. Thermalloy #2328B Pin-Fin Heat Sink-to-Ambient Thermal Resistance vs. Airflow Velocity



Assuming an air velocity of 0.5m/s, we have an effective θ_{SA} of 7°C/W, thus

$T_J = 30°C + 5°C + (2.2°C/W + 1.0°C/W + 7°C/W) \times 4.5W$,

resulting in a junction temperature of approximately 81°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Aavid, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final chip-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power dissipation, a number of factors affect the final operating die-junction temperature. These factors might include air flow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, next-level interconnect technology, system air temperature rise, and so forth.

5.9 Operational and Design Considerations

5.9.1 Level Protection

A level protection feature is included in the PowerPC 750FX RISC Microprocessor. The level protection feature is available in the 1.8V, 2.5V and 3.3V bus modes. This feature prevents ambiguous floating reference voltages by pulling the respective signal line to the last valid or nearest valid state.

For example, if the Input/Output voltage level is closer to OV_{DD}, the circuit pulls the I/O level to $OV_{DD.}$ If the I/O level is closer to GND, the I/O level is pulled low. This self-latching circuitry “keeps” the floating inputs defined and avoids meta-stability. In Table 5-6, these signals are defined as “keeper” in the "Level Protect" column.

The level protect circuitry provides no additional leakage current to the signal I/O; however, some amount of current must be applied to the “keeper” node to overcome the level protection latch. This current is process dependent, but in no case is the current required over 100µA.

This feature allows the system designer to limit the number of resistors in the design and optimize placement and reduce costs.

Note: Having a “keeper” on the associated signal I/O does not replace a pull-up or pull-down resistor that is needed by a separate device located on the 60x bus. The designer must supply any termination requirements for these separate devices. as defined in their specifications.

5.9.2 64 or 32-Bit Data Bus Mode

This mode selection varies for different design revision (DD) levels. The typical operation for the 750FX DD2.X Revision is considered to be in 64-bit Data Bus mode. Mode setting is determined by the state of the mode signal TLBISYNC, at the transition of HRESET from its active to inactive state (low to high). If TLBISYNC is **high** when HRESET transitions from active to inactive, 64-bit mode is selected. If TLBISYNC is **low** when HRESET transitions from active to inactive, 32-bit mode is selected.

Special Note: (Reduced pin out mode) To transition from a previous processor with reduced pin out mode, the customer will need to drive TLBISYNC appropriately, leave the DP(0..7) and AP(0..3) pins floating and disable parity checking with the HID0 bits. The 750FX, like the 750CXe and 750, does not have APE and DPE pins.

5.9.3 I/O Voltage Mode Selection

Selection between 1.8V, 2.5V or 3.3V I/O is accomplished by using the BVSEL and L1_TSTCLK pins:

If BVSEL = 1 and L1_TSTCLK = 0, then the 3.3V mode is enabled.

If BVSEL = 1 and L1_TSTCLK = 1, then the 2.5V mode is enabled.

If BVSEL = 0 and L1_TSTCLK = 1, then the 1.8V mode is enabled.

Note: Do not set BVSEL = 0 and L1_TSTCLK = 0 since it yields an INVALID MODE.

Table 5-10. Summary of Mode Select

	750FX (DD2.x)
32-bit mode	Sample $\overline{\text{TLBISYNC}}$ to select HIGH = 64-bit mode LOW = 32-bit mode
I/O selection	3.3V ± 165mV (BVSEL = 1, L1_TSTCLK = 0) or 2.5V ± 125mV (BVSEL = 1, L1_TSTCLK = 1) or 1.8V ± 100mV (BVSEL = 0, L1_TSTCLK = 1)[1]
Notes: 1. 1.2 -1.5V I/O modes are not supported in this revision.	

This document contains information on products in the sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

Revision Log

The following table lists the revisions to this datasheet.

Date	Description
August 23, 2002	Version 0.1 Initial preliminary, IBM Confidential version.
August 29, 2002	Version 0.2 Preliminary, IBM Confidential version. • *Table 4-3 Signal Listing for the CBGA Package* - Updated note for $\overline{\text{TLBISYNC}}$: high = 64-bit mode, low =32-bit mode.